FIG. 1

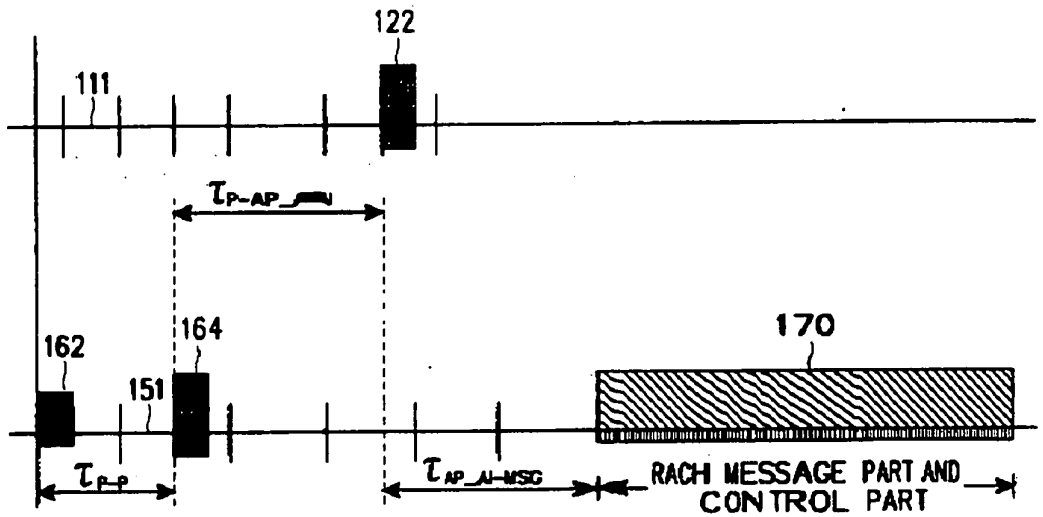

122
111
τ_{P-AP}
162
164
151
170
τ_{P-P}
τ_{AP_AI-MSG}
RACH MESSAGE PART AND
CONTROL PART

FIG_ 2

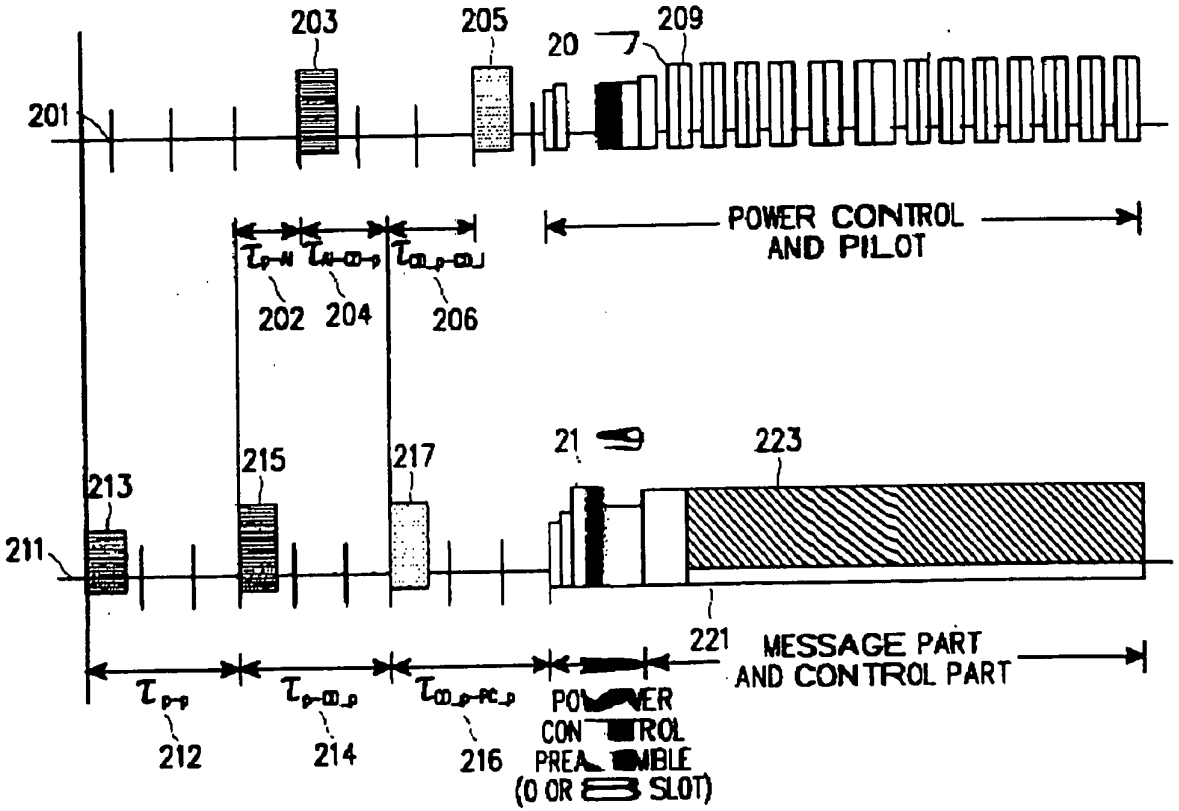

203
205
209
201
POWER CONTROL
AND PILOT
202
204
206
213
215
217
223
211
221
MESSAGE PART
AND CONTROL PART
212
214
216
(0 OR 8 SLOT)

FIG. 3

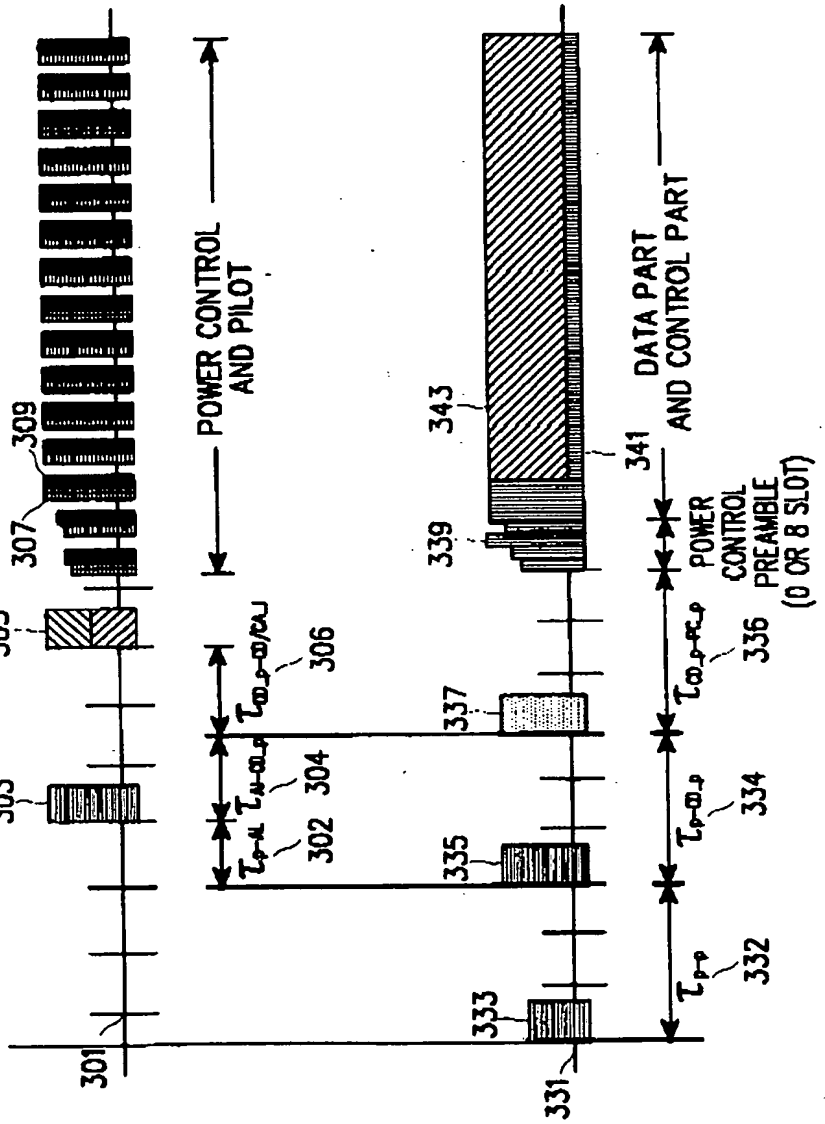
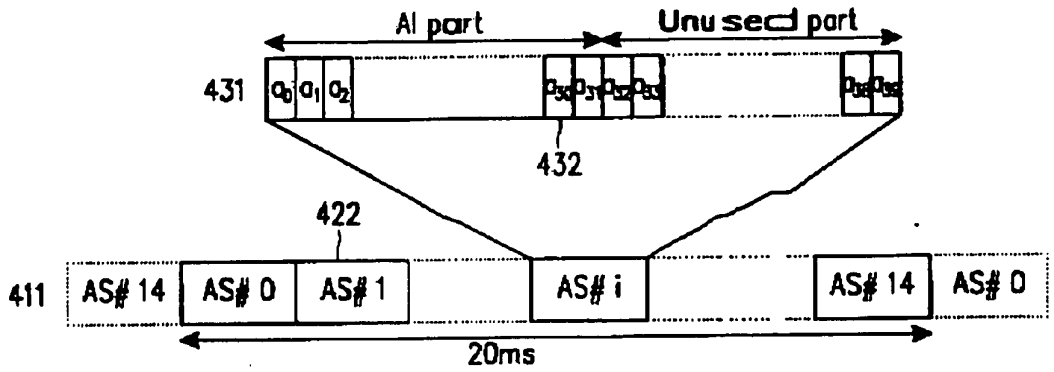

301
303
305
307
309
POWER CONTROL AND PILOT
302
304
306
331
333
335
337
339
341
343
DATA PART AND CONTROL PART
POWER CONTROL PREAMBLE (0 OR 8 SLOT)
332
334
336

FIG. 4


AI part
Unused part
431
a_0 a_1 a_2
a_{39} a_{38} a_{37} a_{36}
a_{191} a_{190}
432
422
411
AS# 14
AS# 0
AS# 1
AS# i
AS# 14
AS# 0
20ms

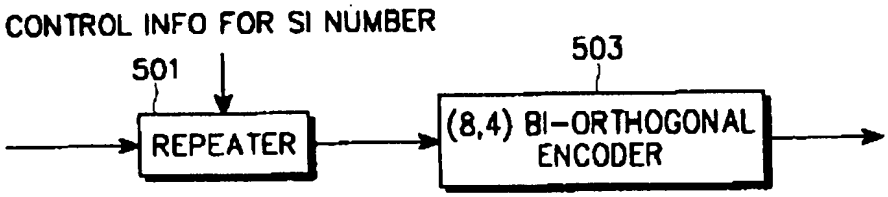

CONTROL INFO FOR SI NUMBER
501
503
REPEATER
(8,4) BI-ORTHOGONAL ENCODER

FIG. 5

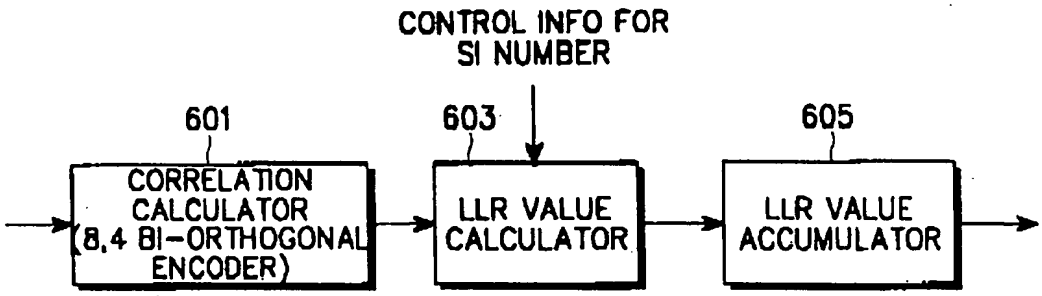
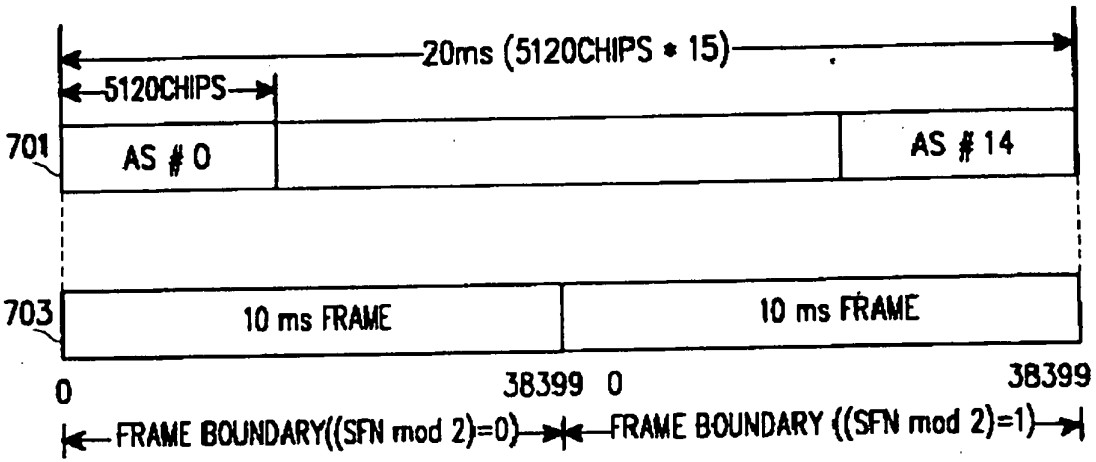

CONTROL INFO FOR
SI NUMBER
601
603
605
CORRELATION
CALCULATOR
(8,4 BI-ORTHOGONAL
ENCODER)
LLR VALUE
CALCULATOR
LLR VALUE
ACCUMULATOR

FIG. 6

FIG. 7


20ms (5120CHIPS * 15)
5120CHIPS
701
AS # 0
AS # 14
703
10 ms FRAME
10 ms FRAME
0
38399
0
38399
FRAME BOUNDARY((SFN mod 2)=0)
FRAME BOUNDARY ((SFN mod 2)=1)

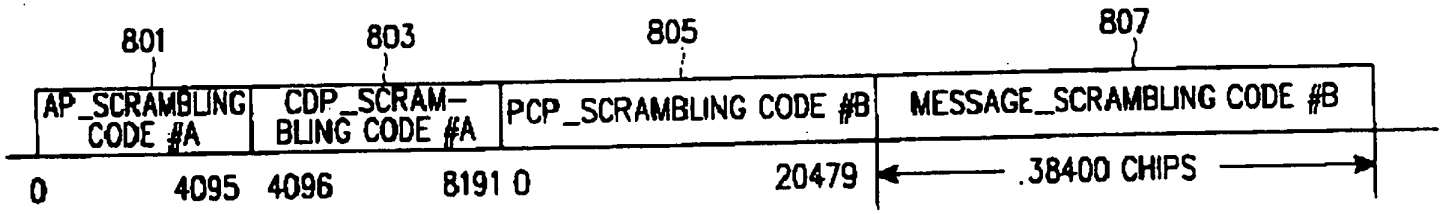

801
803
805
807
AP_SCRAMBLING CODE #A
CDP_SCRAM-BLING CODE #A
PCP_SCRAMBLING CODE #B
MESSAGE_SCRAMBLING CODE #B
0
4095
4096
8191
0
20479
38400 CHIPS

FIG. 8A

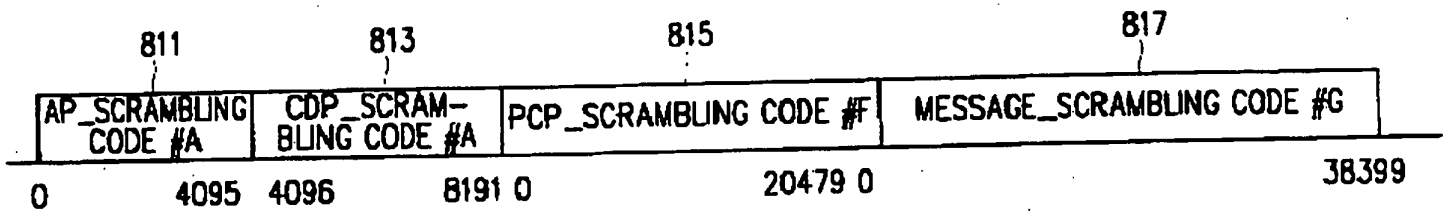

811
813
815
817
AP_SCRAMBLING CODE #A
CDP_SCRAM-BLING CODE #A
PCP_SCRAMBLING CODE #F
MESSAGE_SCRAMBLING CODE #G
0
4095
4096
8191
0
20479
0
38399

FIG. 8B

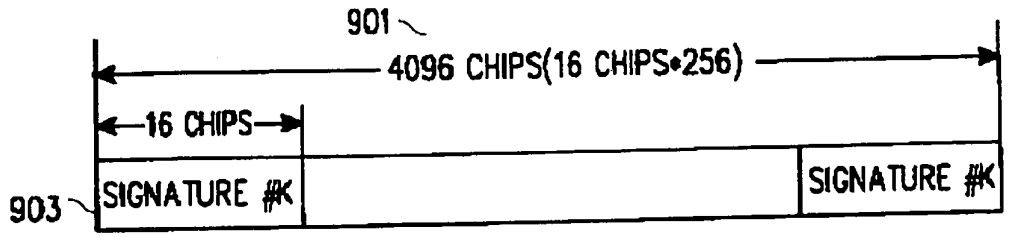

901
4096 CHIPS(16 CHIPS•256)
16 CHIPS
SIGNATURE #K
SIGNATURE #K
903

FIG. 9A

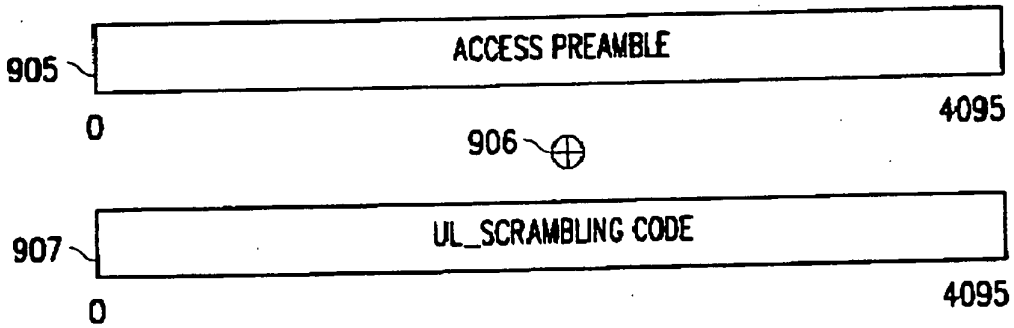

905
ACCESS PREAMBLE
0
4095
906
907
UL_SCRAMBLING CODE
0
4095

FIG. 9B

FIG. 10A

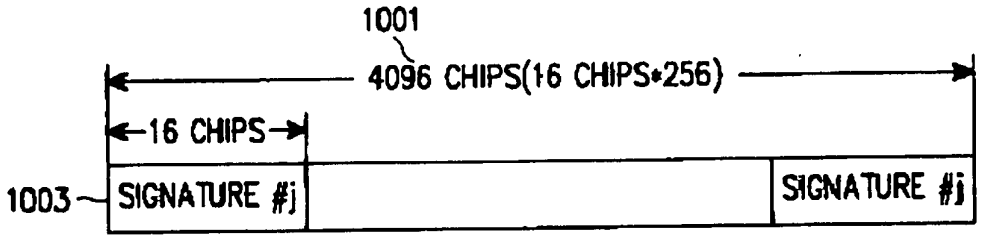
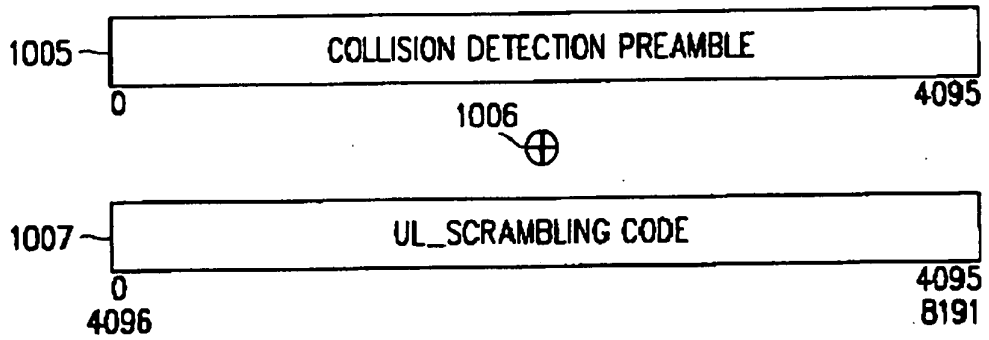


FIG. 10B



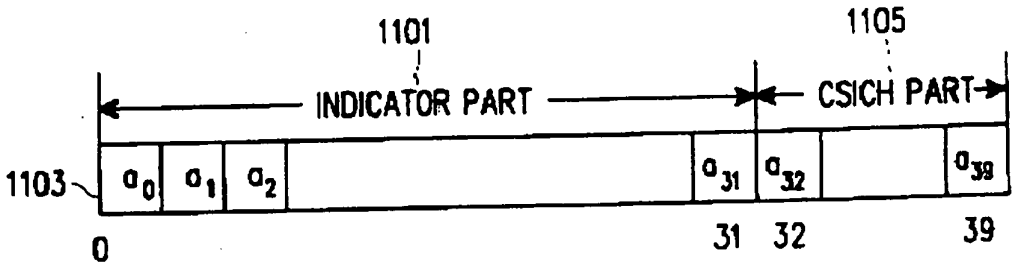


FIG. 11A

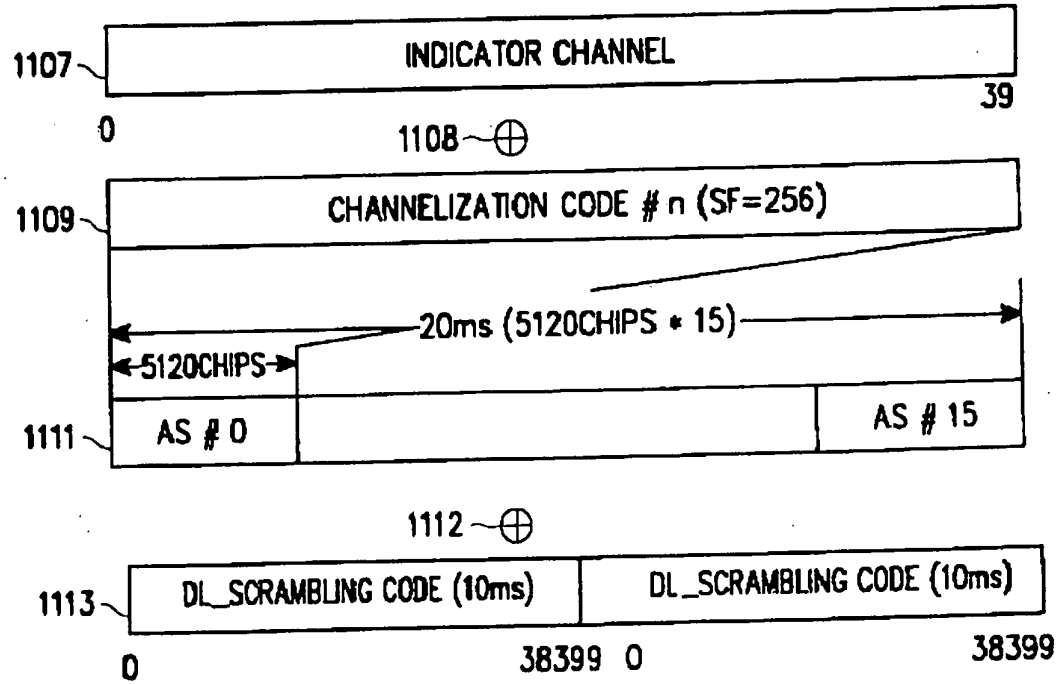


FIG. 11B

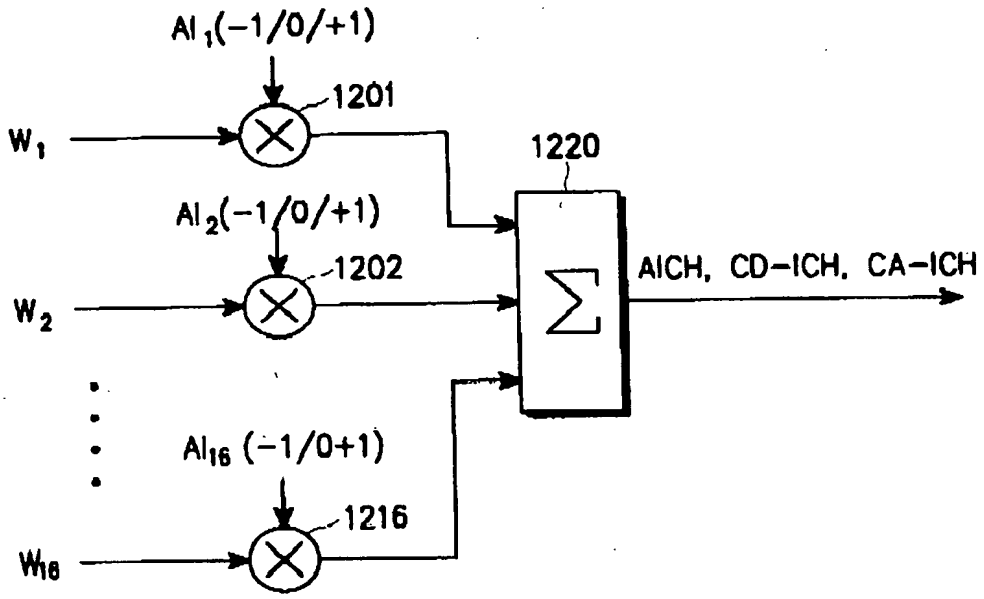

AI1(−1/0/+1)
1201
W1
1220
AI2(−1/0/+1)
1202
W2
AICH, CD−ICH, CA−ICH
AI16 (−1/0+1)
1216
W16

FIG. 12

FIG. 13A

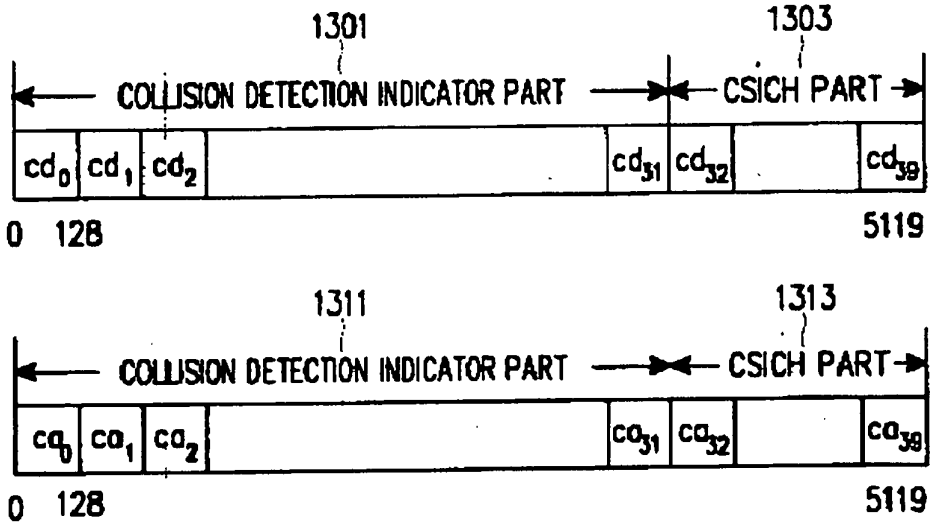
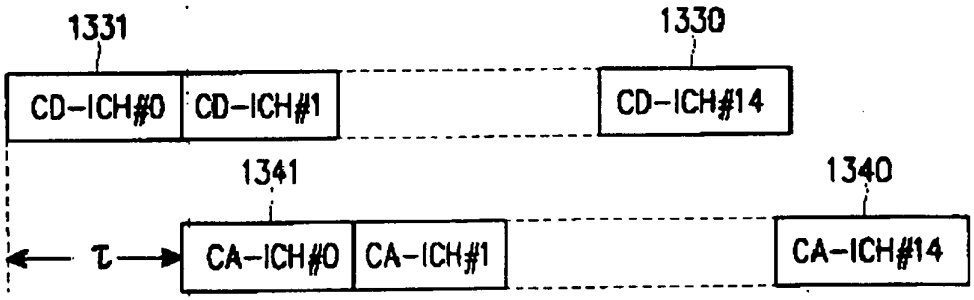


FIG. 13B



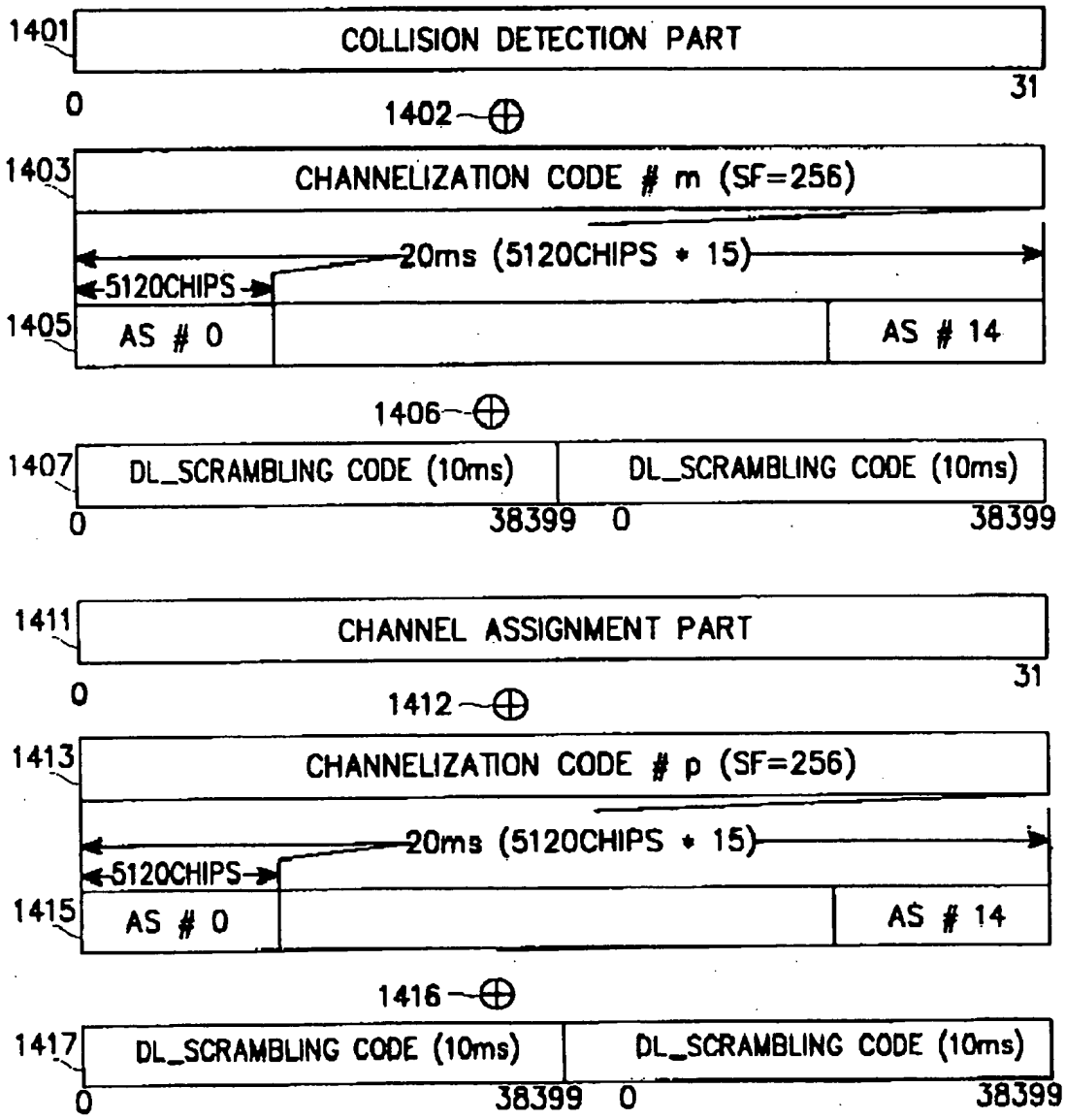

1401
COLLISION DETECTION PART
0
31
1402
1403
CHANNELIZATION CODE # m (SF=256)
20ms (5120CHIPS * 15)
5120CHIPS
1405
AS # 0
AS # 14
1406
1407
DL_SCRAMBLING CODE (10ms)
DL_SCRAMBLING CODE (10ms)
0
38399
0
38399
1411
CHANNEL ASSIGNMENT PART
0
31
1412
1413
CHANNELIZATION CODE # p (SF=256)
20ms (5120CHIPS * 15)
5120CHIPS
1415
AS # 0
AS # 14
1416
1417
DL_SCRAMBLING CODE (10ms)
DL_SCRAMBLING CODE (10ms)
0
38399
0
38399

FIG. 14

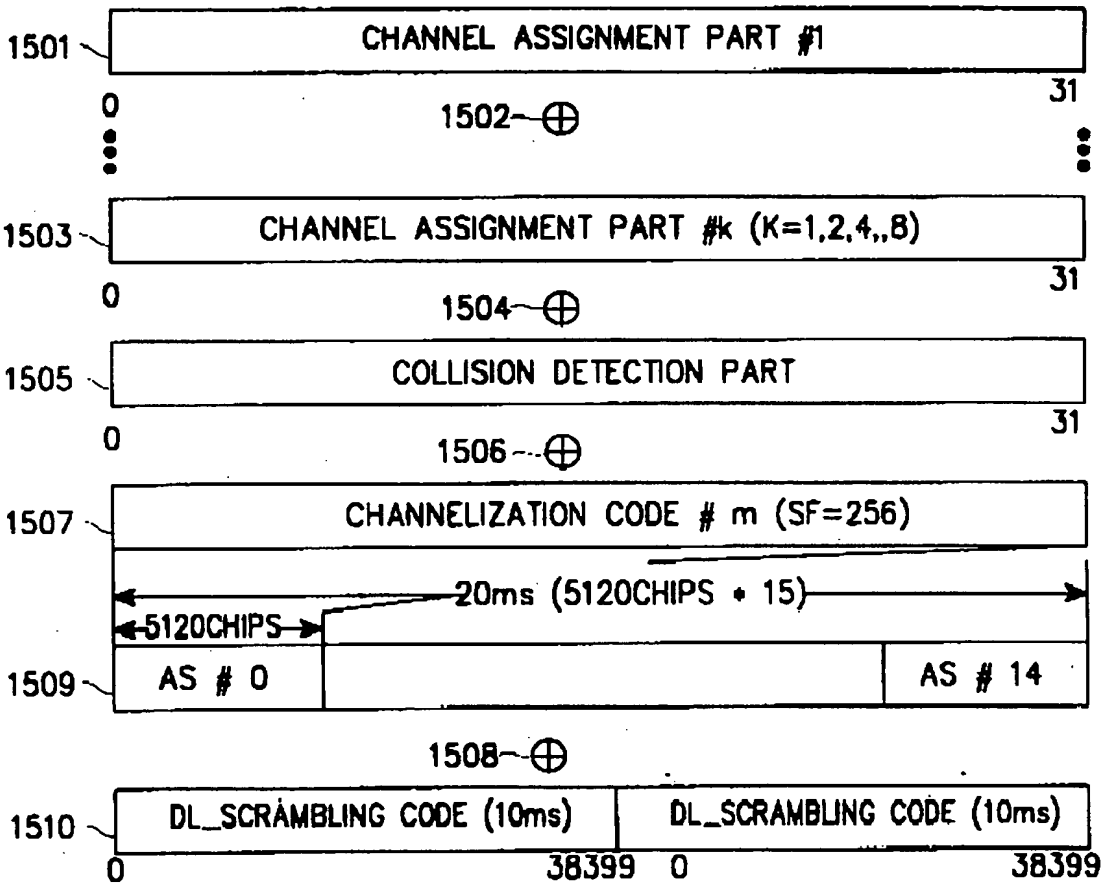

1501
CHANNEL ASSIGNMENT PART #1
0
31
1502
1503
CHANNEL ASSIGNMENT PART #k (K=1,2,4,,8)
0
31
1504
1505
COLLISION DETECTION PART
0
31
1506
1507
CHANNELIZATION CODE # m (SF=256)
20ms (5120CHIPS * 15)
5120CHIPS
1509
AS # 0
AS # 14
1508
1510
DL_SCRAMBLING CODE (10ms)
DL_SCRAMBLING CODE (10ms)
0
38399
0
38399

FIG. 15

FIG. 16

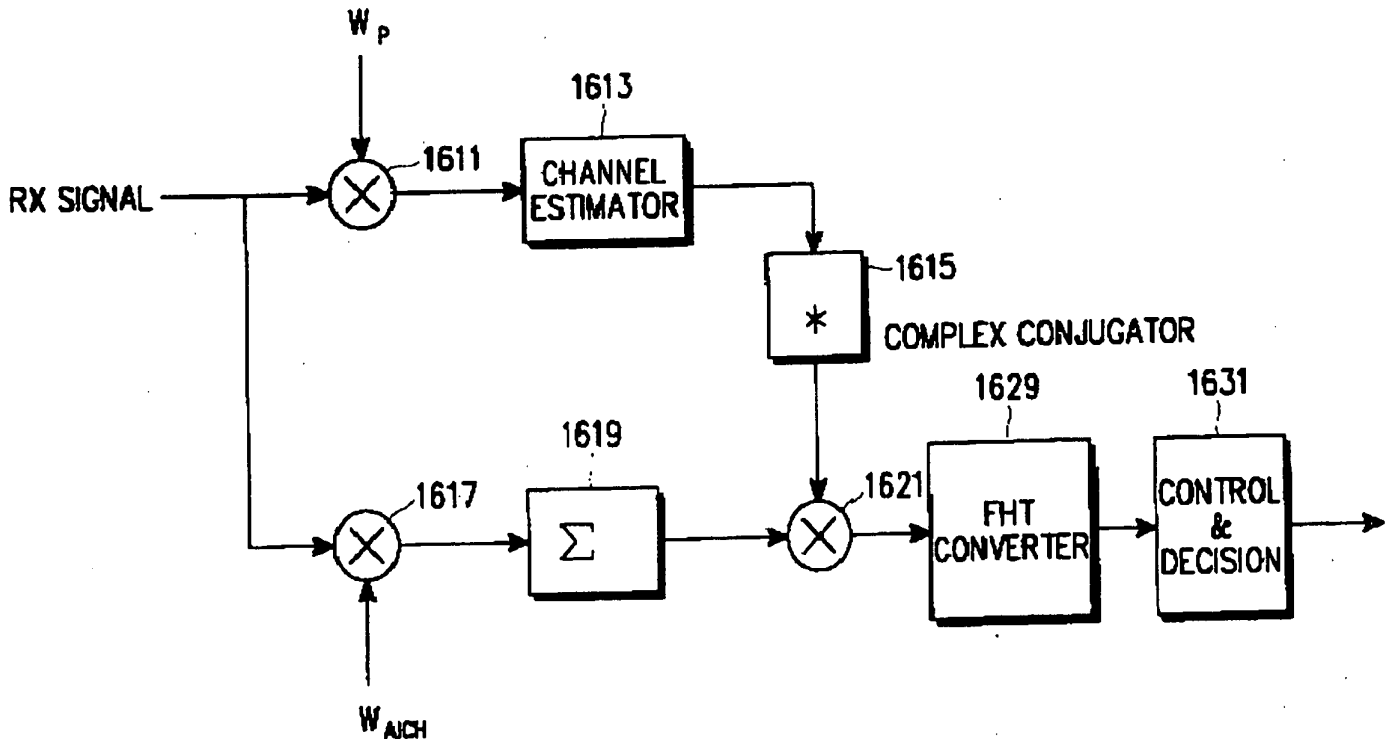
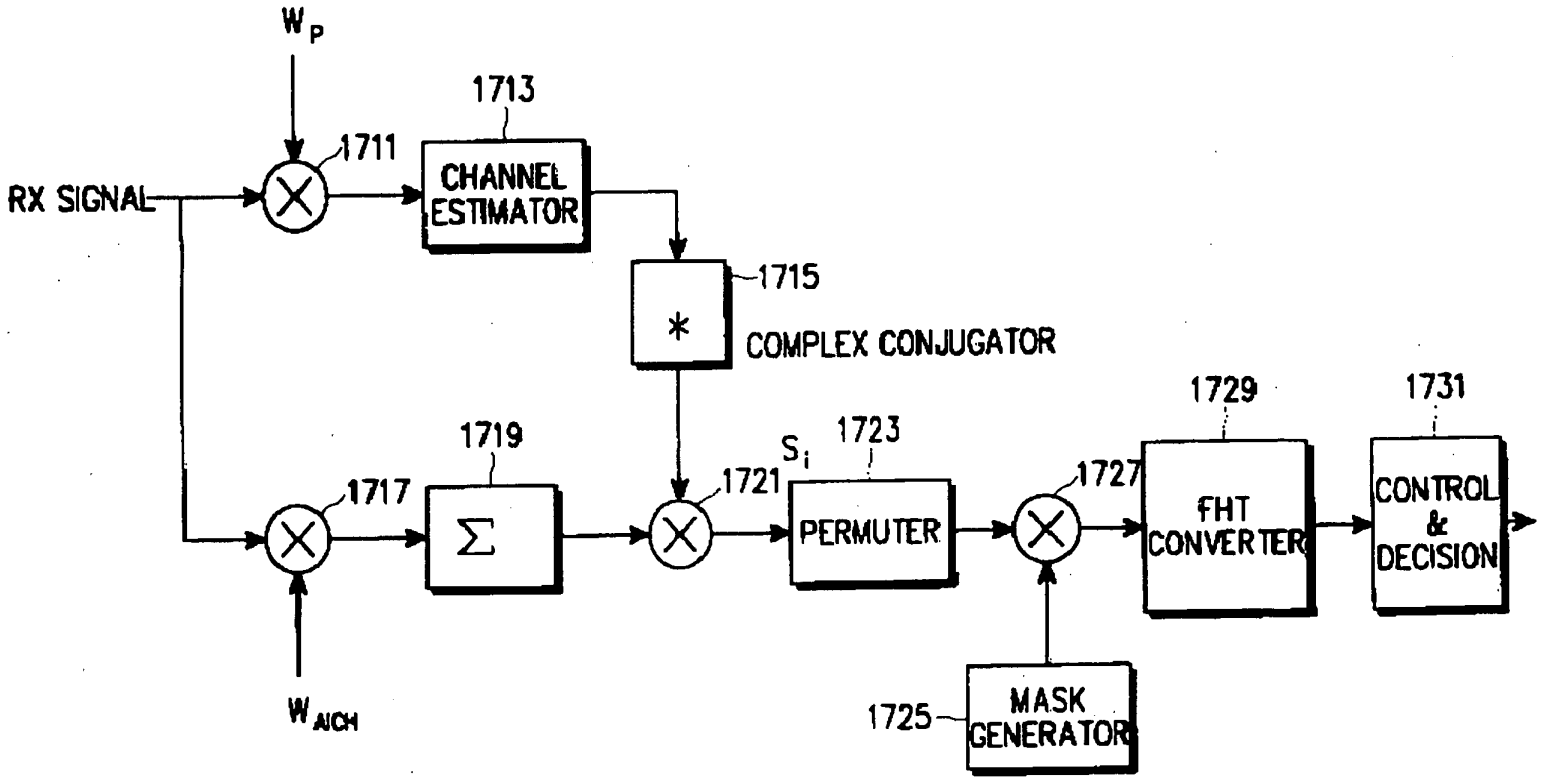

W P
1613
1611
RX SIGNAL
CHANNEL ESTIMATOR
1615
*
COMPLEX CONJUGATOR
1629
1631
1619
1617
1621
Σ
FHT CONVERTER
CONTROL & DECISION
W AICH

FIG. 17


W P
1713
1711
RX SIGNAL
CHANNEL ESTIMATOR
1715
*
COMPLEX CONJUGATOR
1729
1731
1719
S i
1723
1717
1721
1727
Σ
PERMUTER
FHT CONVERTER
CONTROL & DECISION
W AICH
1725
MASK GENERATOR

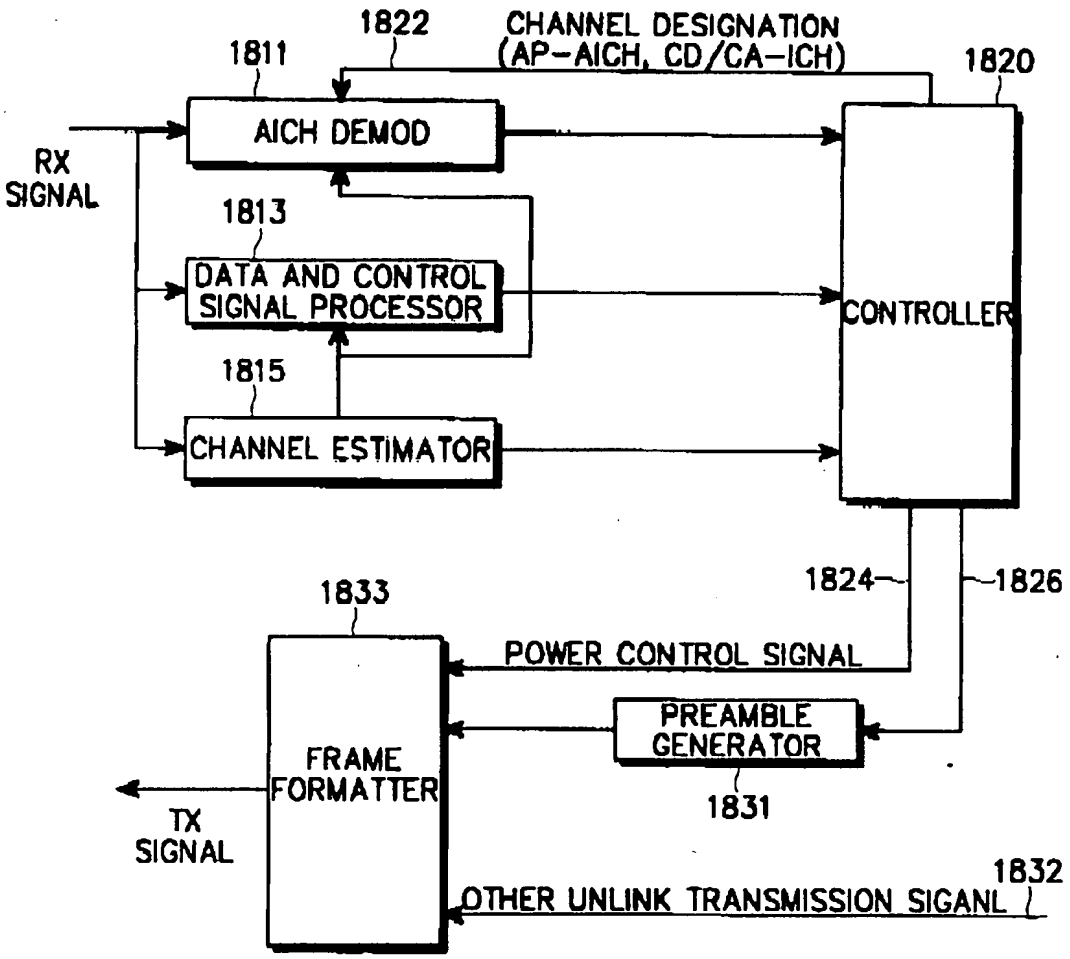

1822
CHANNEL DESIGNATION
(AP-AICH, CD/CA-ICH)
1811
1820
AICH DEMOD
RX
SIGNAL
1813
DATA AND CONTROL
SIGNAL PROCESSOR
CONTROLLER
1815
CHANNEL ESTIMATOR
1824
1826
1833
POWER CONTROL SIGNAL
PREAMBLE
GENERATOR
FRAME
FORMATTER
1831
TX
SIGNAL
1832
OTHER UNLINK TRANSMISSION SIGANL

FIG. 18

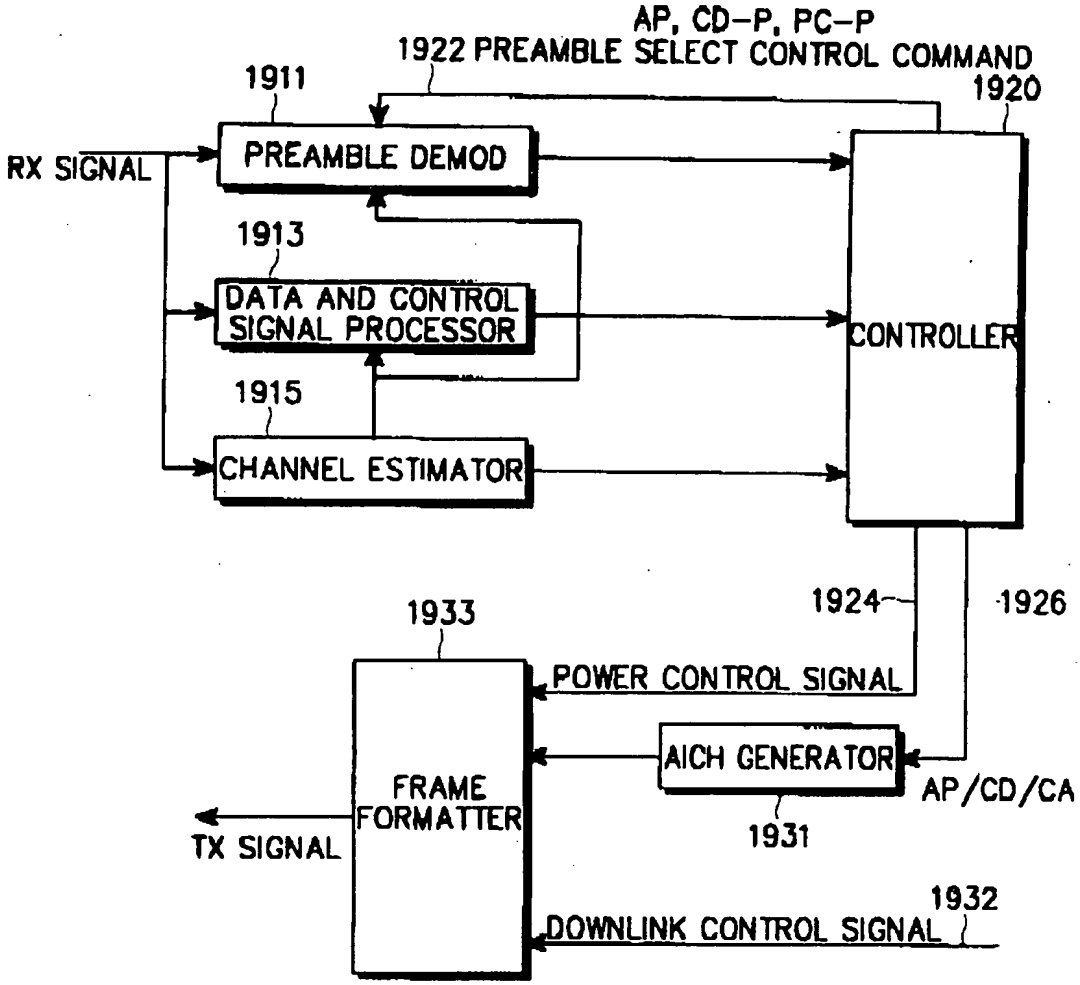

AP, CD-P, PC-P
1922 PREAMBLE SELECT CONTROL COMMAND
1911
1920
RX SIGNAL
PREAMBLE DEMOD
1913
DATA AND CONTROL SIGNAL PROCESSOR
CONTROLLER
1915
CHANNEL ESTIMATOR
1924
1926
1933
POWER CONTROL SIGNAL
AICH GENERATOR
AP/CD/CA
FRAME FORMATTER
TX SIGNAL
1931
1932
DOWNLINK CONTROL SIGNAL

FIG. 19

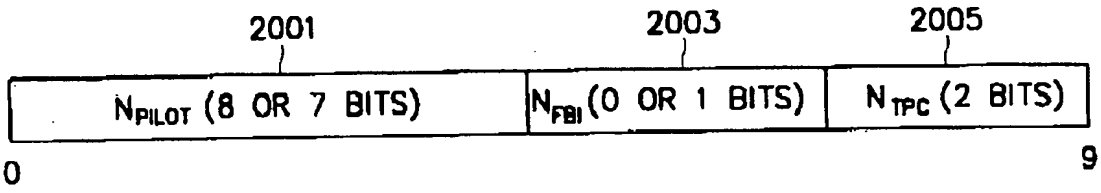


FIG. 20

FIG. 21

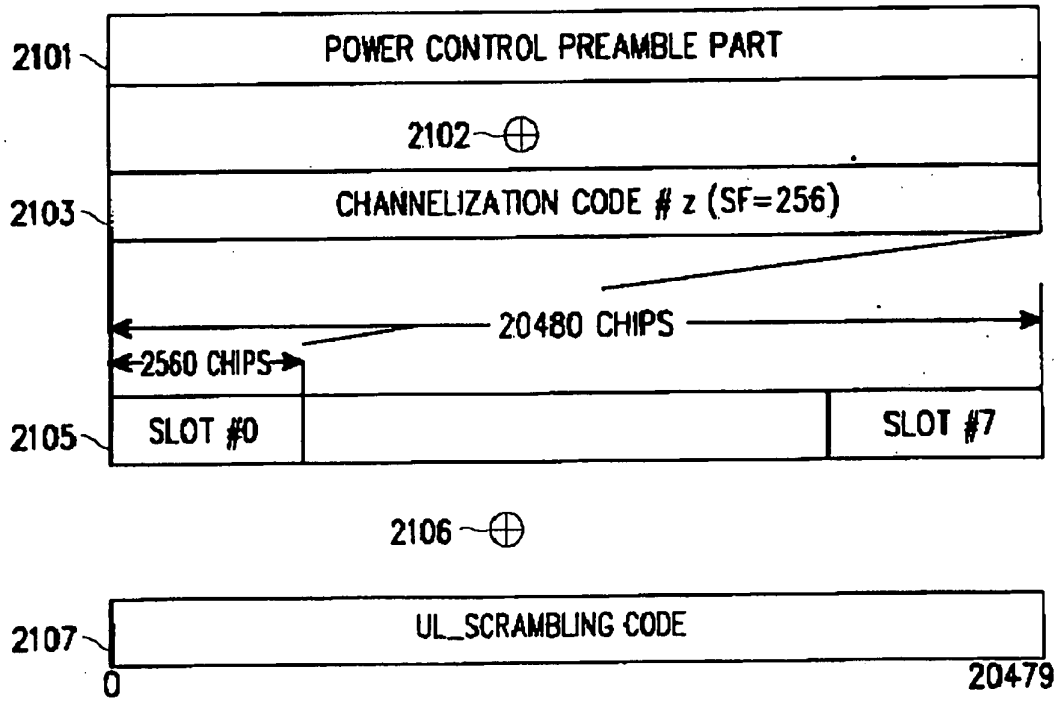

2101
POWER CONTROL PREAMBLE PART
2102
2103
CHANNELIZATION CODE # z (SF=256)
20480 CHIPS
2560 CHIPS
2105
SLOT #0
SLOT #7
2106
2107
UL_SCRAMBLING CODE
0
20479

FIG. 22A

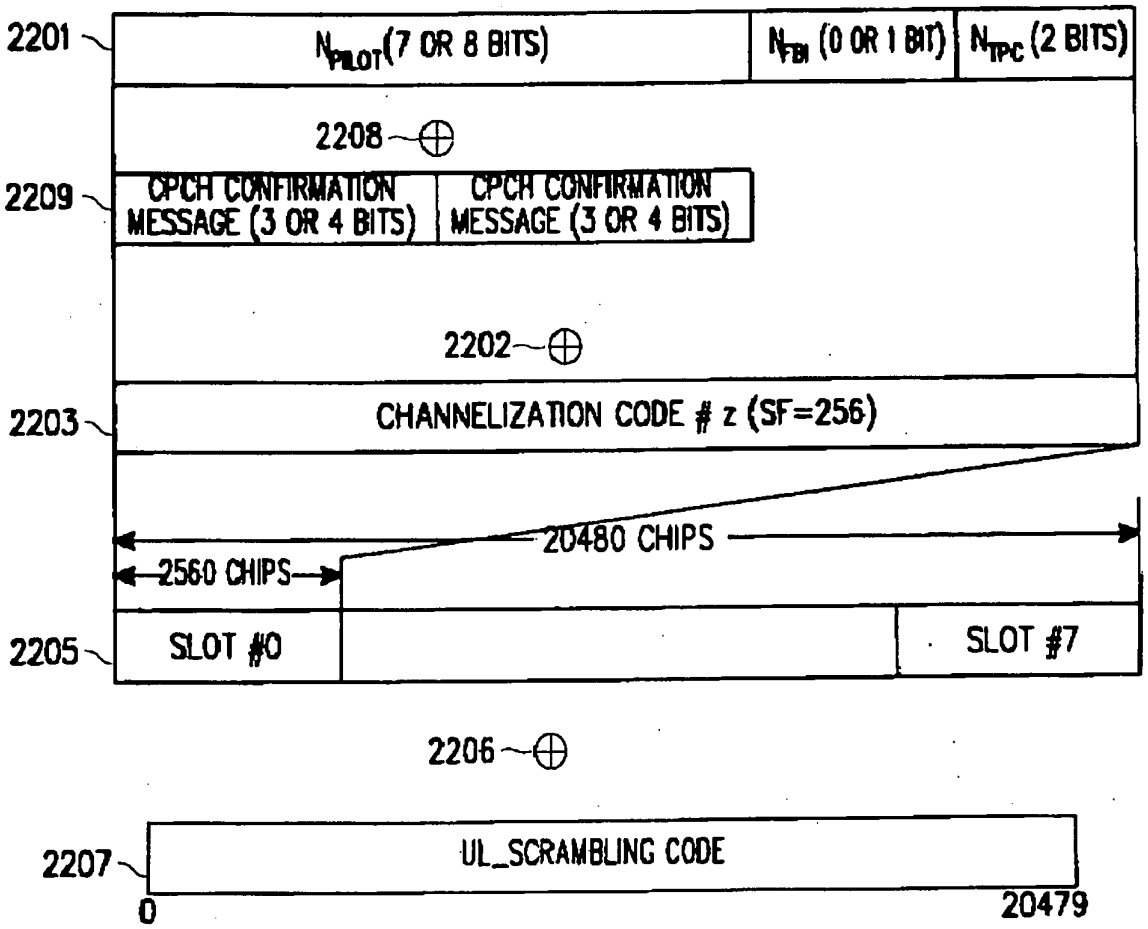

2201
N_{PILOT}(7 OR 8 BITS)
N_{FBI} (0 OR 1 BIT)
N_{TPC} (2 BITS)
2208
2209
CPCH CONFIRMATION MESSAGE (3 OR 4 BITS)
CPCH CONFIRMATION MESSAGE (3 OR 4 BITS)
2202
2203
CHANNELIZATION CODE # z (SF=256)
20480 CHIPS
2560 CHIPS
2205
SLOT #0
SLOT #7
2206
2207
UL_SCRAMBLING CODE
0
20479

FIG. 22B

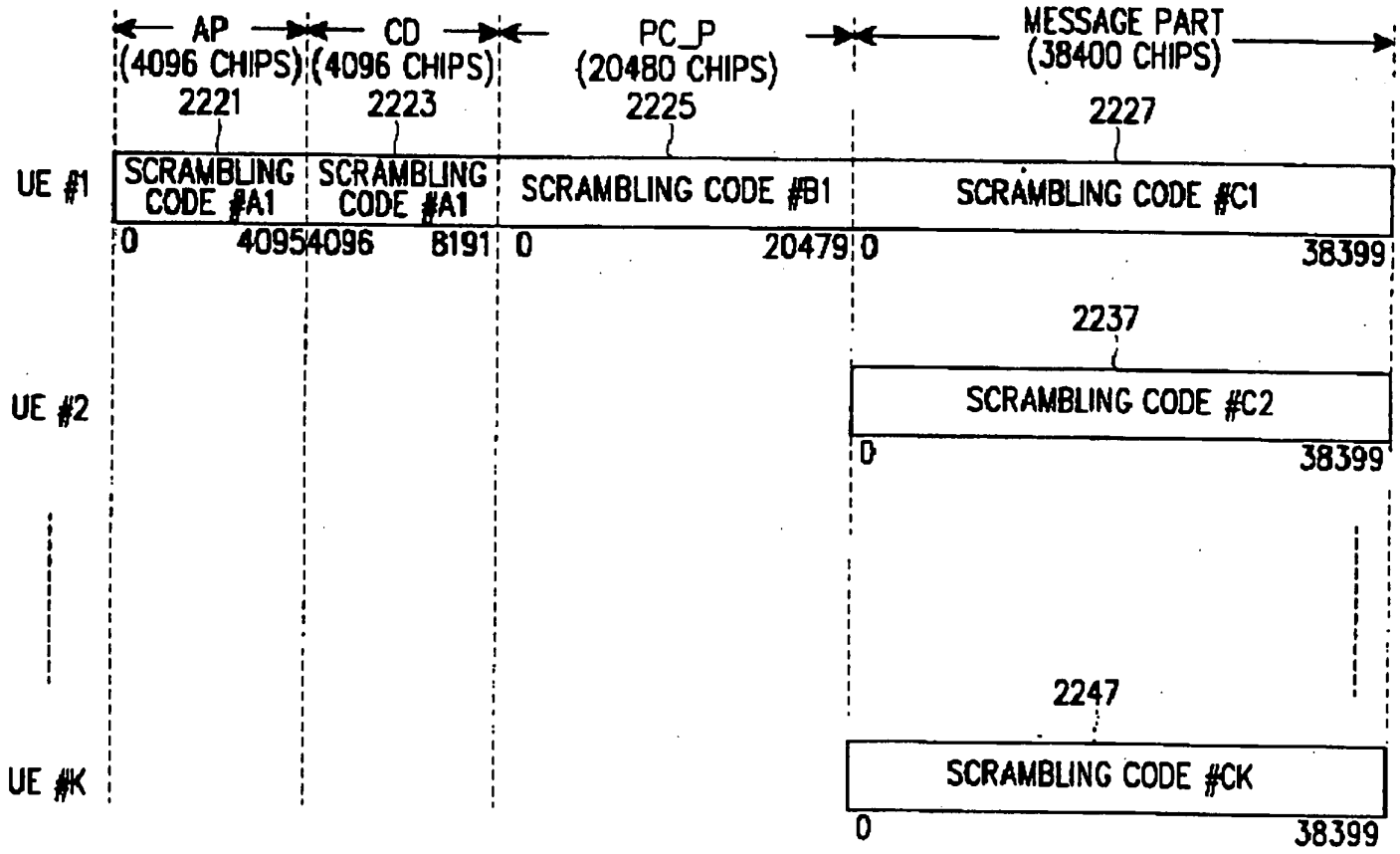

AP
(4096 CHIPS)
CD
(4096 CHIPS)
PC_P
(20480 CHIPS)
MESSAGE PART
(38400 CHIPS)
2221
2223
2225
2227
UE #1
SCRAMBLING CODE #A1
SCRAMBLING CODE #A1
SCRAMBLING CODE #B1
SCRAMBLING CODE #C1
0
4095
4096
8191
0
20479
0
38399
2237
UE #2
SCRAMBLING CODE #C2
0
38399
2247
UE #K
SCRAMBLING CODE #CK
0
38399

FIG. 23

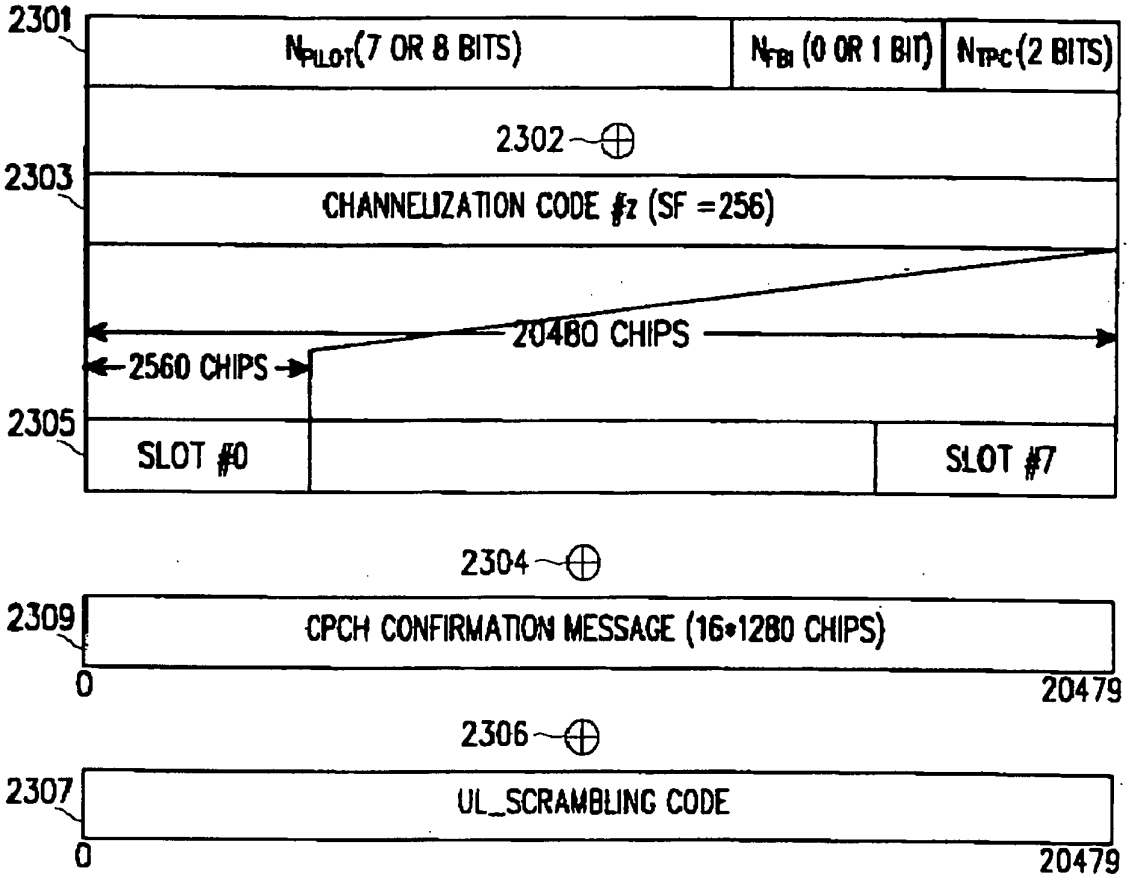

2301
N_{PILOT}(7 OR 8 BITS)
N_{FBI} (0 OR 1 BIT)
N_{TPC}(2 BITS)
2302
2303
CHANNELIZATION CODE #z (SF =256)
20480 CHIPS
2560 CHIPS
2305
SLOT #0
SLOT #7
2304
2309
CPCH CONFIRMATION MESSAGE (16*1280 CHIPS)
0
20479
2306
2307
UL_SCRAMBLING CODE
0
20479

FIG. 24A

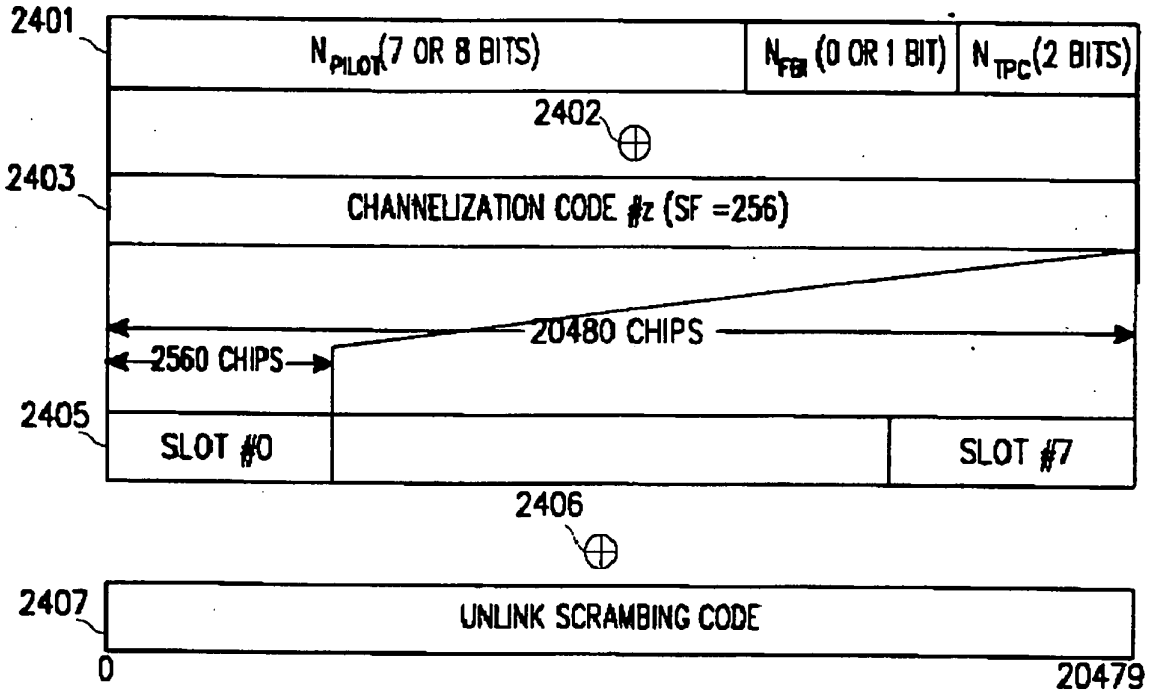

2401
N_{PILOT}(7 OR 8 BITS)
N_{FBI} (0 OR 1 BIT)
N_{TPC}(2 BITS)
2402
2403
CHANNELIZATION CODE #z (SF =256)
20480 CHIPS
2560 CHIPS
2405
SLOT #0
SLOT #7
2406
2407
UNLINK SCRAMBING CODE
0
20479

FIG. 24B

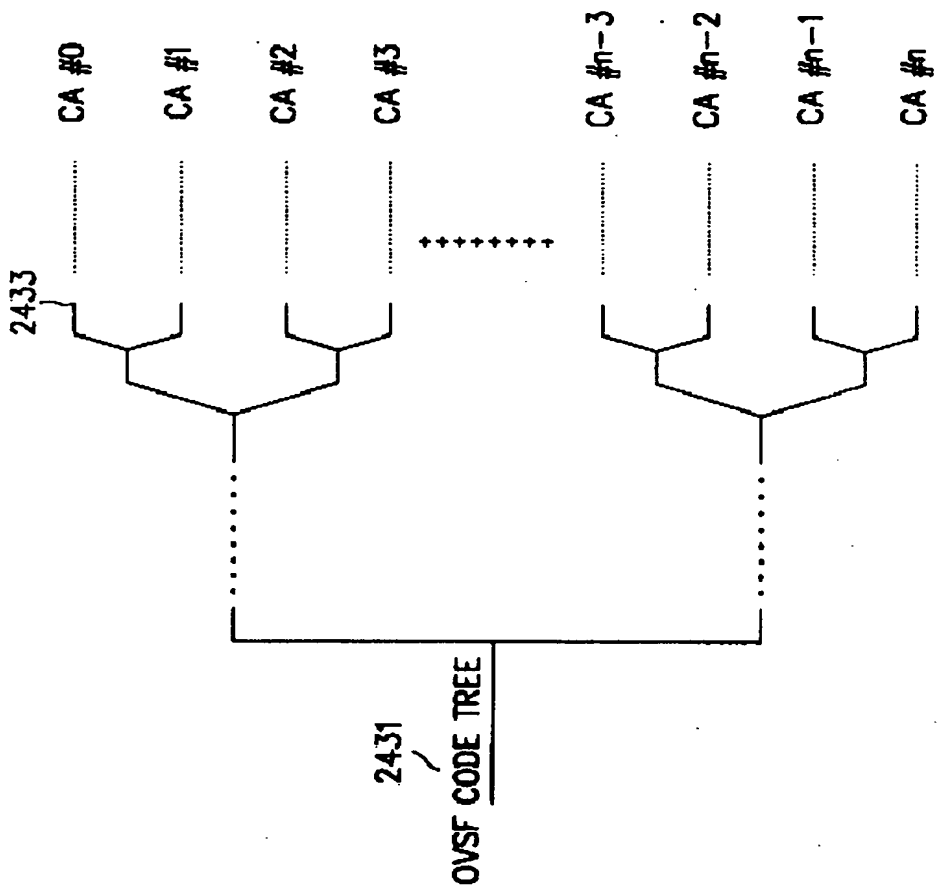


FIG. 25A

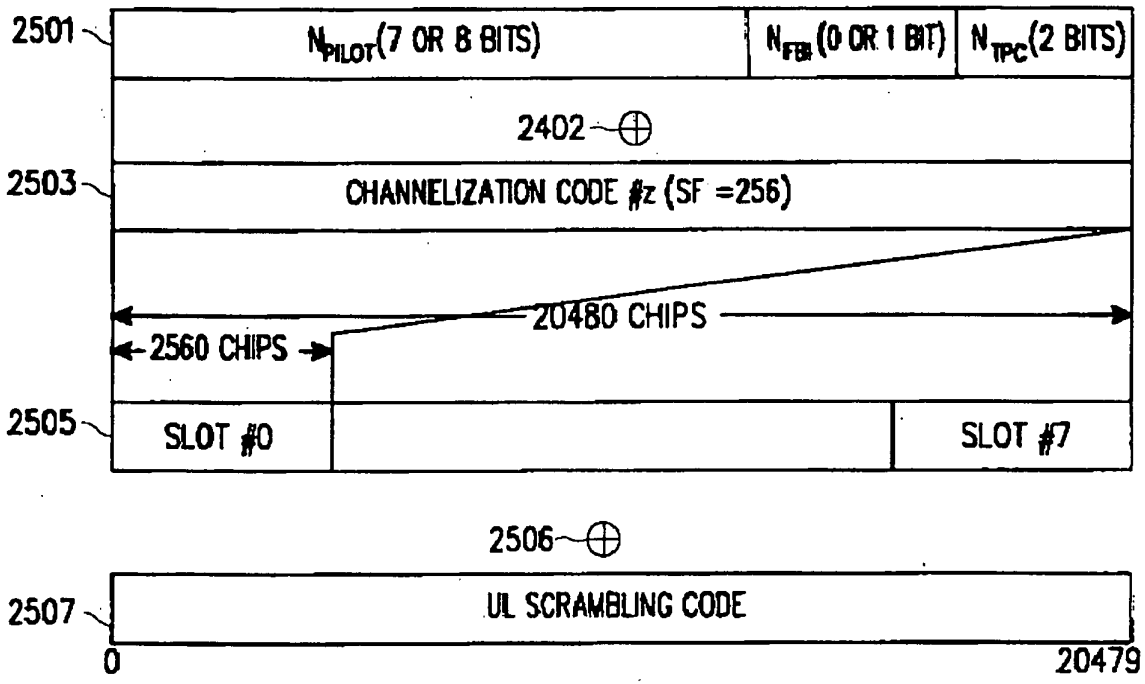
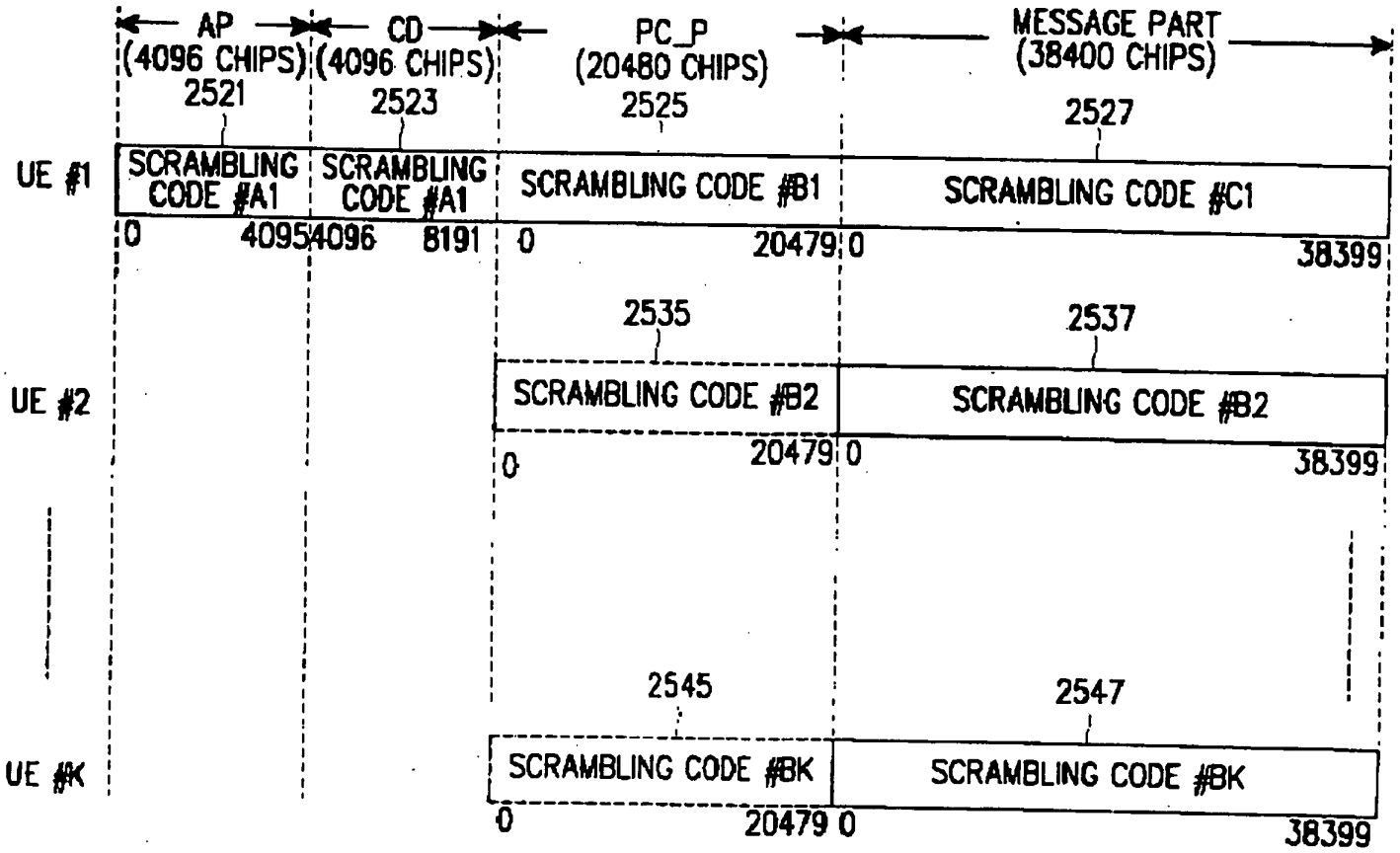

2501
N_{PILOT}(7 OR 8 BITS)
N_{FBI}(0 OR 1 BIT)
N_{TPC}(2 BITS)
2402
2503
CHANNELIZATION CODE #z (SF =256)
20480 CHIPS
2560 CHIPS
2505
SLOT #0
SLOT #7
2506
2507
UL SCRAMBLING CODE
0
20479

FIG. 25B


AP
(4096 CHIPS)
CD
(4096 CHIPS)
PC_P
(20480 CHIPS)
MESSAGE PART
(38400 CHIPS)
2521
2523
2525
2527
UE #1
SCRAMBLING CODE #A1
SCRAMBLING CODE #A1
SCRAMBLING CODE #B1
SCRAMBLING CODE #C1
0
4095
4096
8191
0
20479
0
38399
2535
2537
UE #2
SCRAMBLING CODE #B2
SCRAMBLING CODE #B2
0
20479
0
38399
2545
2547
UE #K
SCRAMBLING CODE #BK
SCRAMBLING CODE #BK
0
20479
0
38399

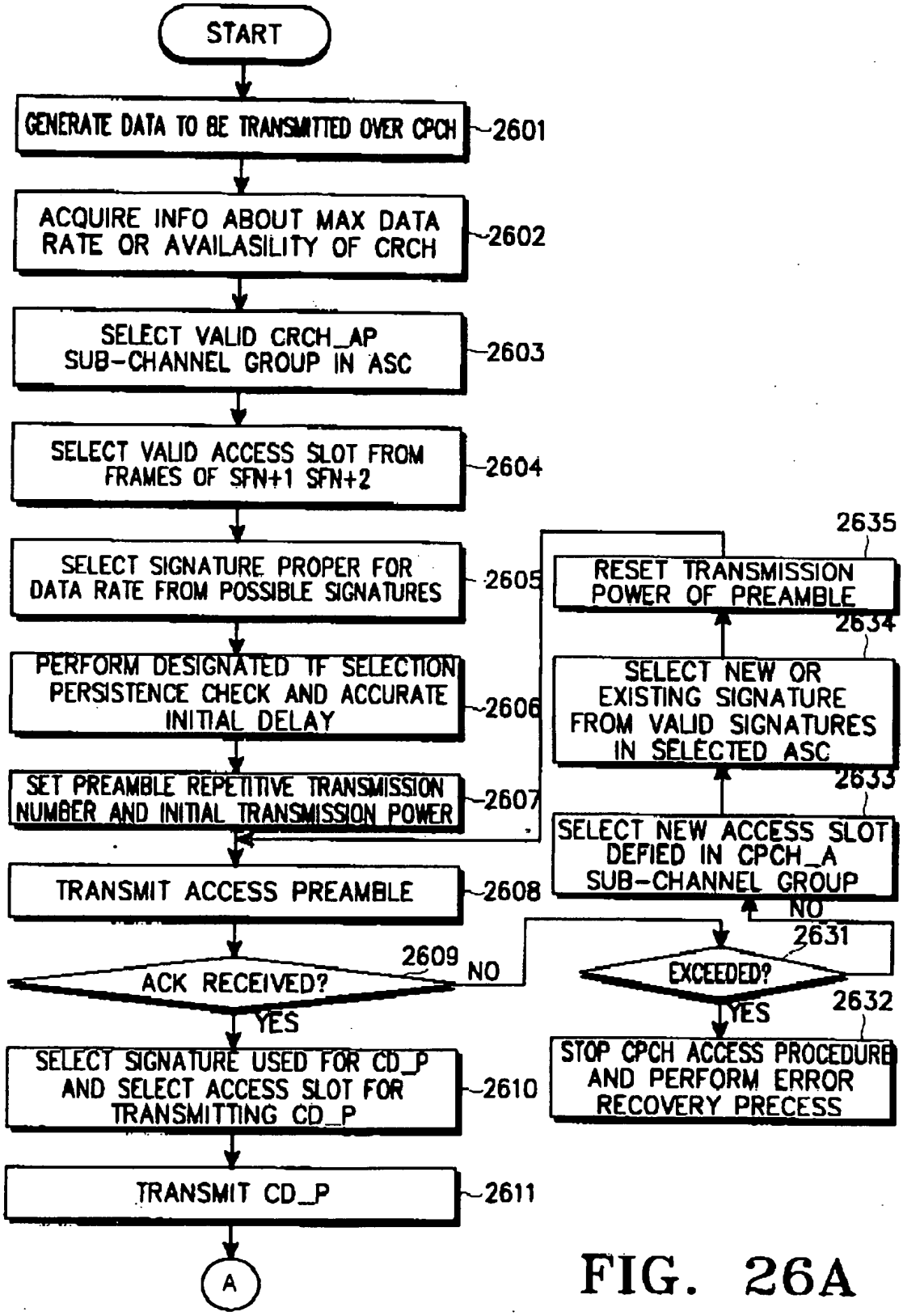

START
GENERATE DATA TO BE TRANSMITTED OVER CPCH
2601
ACQUIRE INFO ABOUT MAX DATA RATE OR AVAILASILITY OF CRCH
2602
SELECT VALID CRCH_AP SUB-CHANNEL GROUP IN ASC
2603
SELECT VALID ACCESS SLOT FROM FRAMES OF SFN+1 SFN+2
2604
SELECT SIGNATURE PROPER FOR DATA RATE FROM POSSIBLE SIGNATURES
2605
PERFORM DESIGNATED TF SELECTION PERSISTENCE CHECK AND ACCURATE INITIAL DELAY
2606
SET PREAMBLE REPETITIVE TRANSMISSION NUMBER AND INITIAL TRANSMISSION POWER
2607
TRANSMIT ACCESS PREAMBLE
2608
ACK RECEIVED?
2609
NO
YES
SELECT SIGNATURE USED FOR CD_P AND SELECT ACCESS SLOT FOR TRANSMITTING CD_P
2610
TRANSMIT CD_P
2611
A
EXCEEDED?
2631
NO
YES
SELECT NEW ACCESS SLOT DEFIED IN CPCH_A SUB-CHANNEL GROUP
2633
SELECT NEW OR EXISTING SIGNATURE FROM VALID SIGNATURES IN SELECTED ASC
2634
RESET TRANSMISSION POWER OF PREAMBLE
2635
STOP CPCH ACCESS PROCEDURE AND PERFORM ERROR RECOVERY PRECESS
2632

FIG. 26A

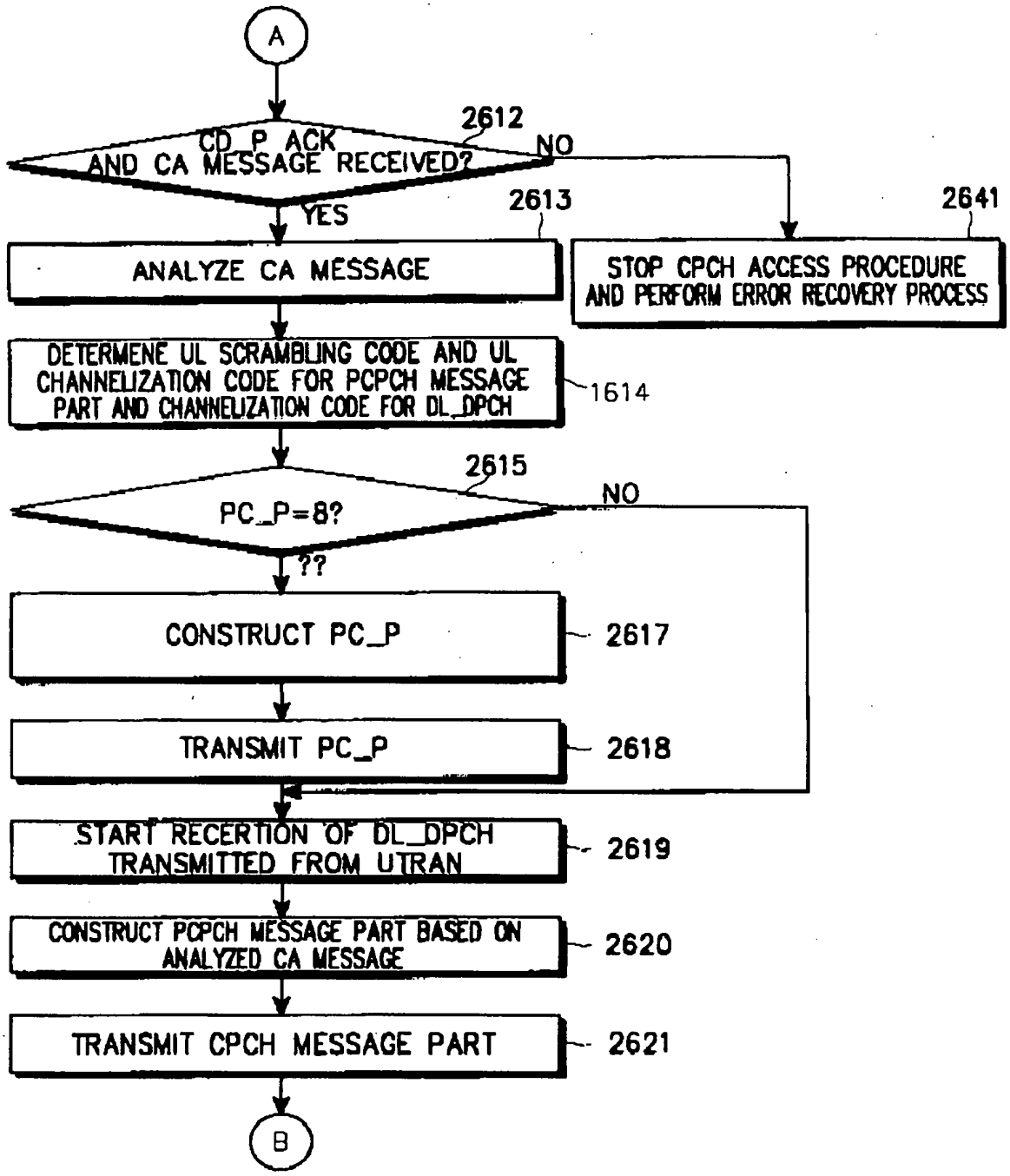

A
CD_P ACK AND CA MESSAGE RECEIVED?
2612
NO
YES
2613
2641
ANALYZE CA MESSAGE
STOP CPCH ACCESS PROCEDURE AND PERFORM ERROR RECOVERY PROCESS
DETERMENE UL SCRAMBLING CODE AND UL CHANNELIZATION CODE FOR PCPCH MESSAGE PART AND CHANNELIZATION CODE FOR DL_DPCH
1614
2615
PC_P=8?
NO
??
CONSTRUCT PC_P
2617
TRANSMIT PC_P
2618
START RECERTION OF DL_DPCH TRANSMITTED FROM UTRAN
2619
CONSTRUCT PCPCH MESSAGE PART BASED ON ANALYZED CA MESSAGE
2620
TRANSMIT CPCH MESSAGE PART
2621
B

FIG. 26B

FLOWCHART OF CPCH USING CHANNEL ASSIGNMENT
(UE SIDE)

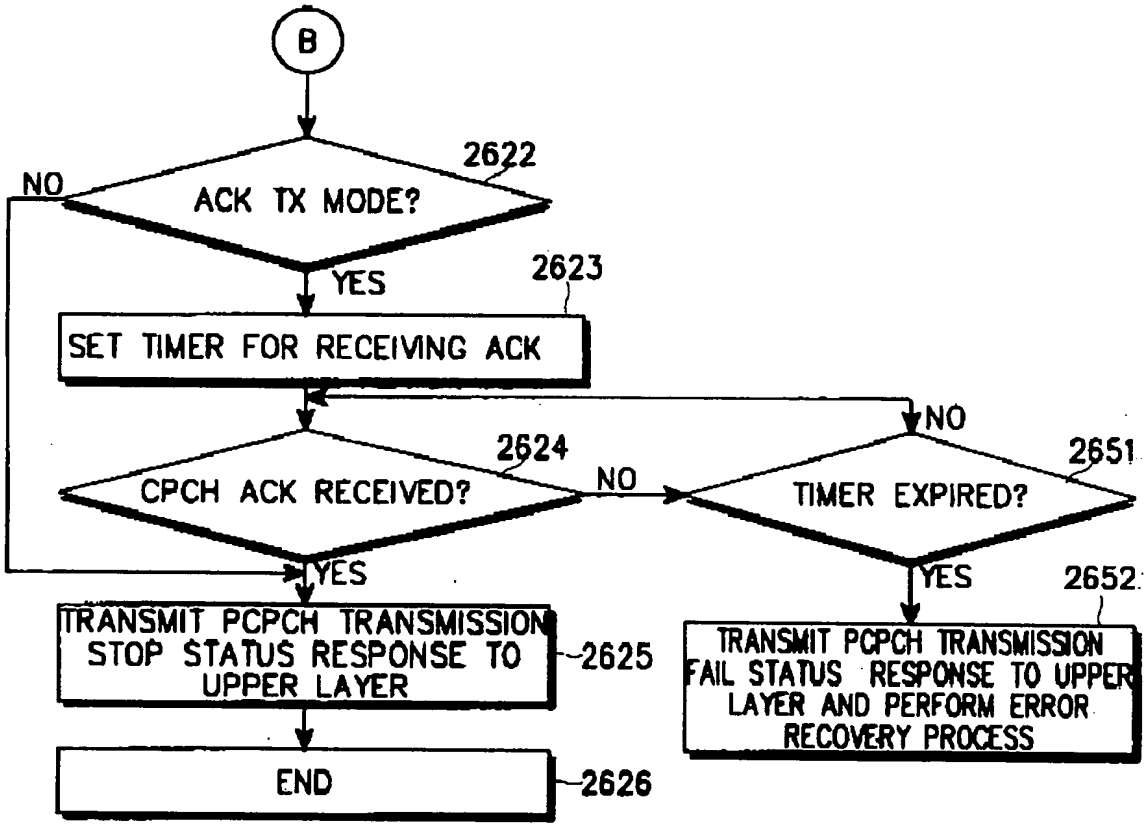


FIG. 26C

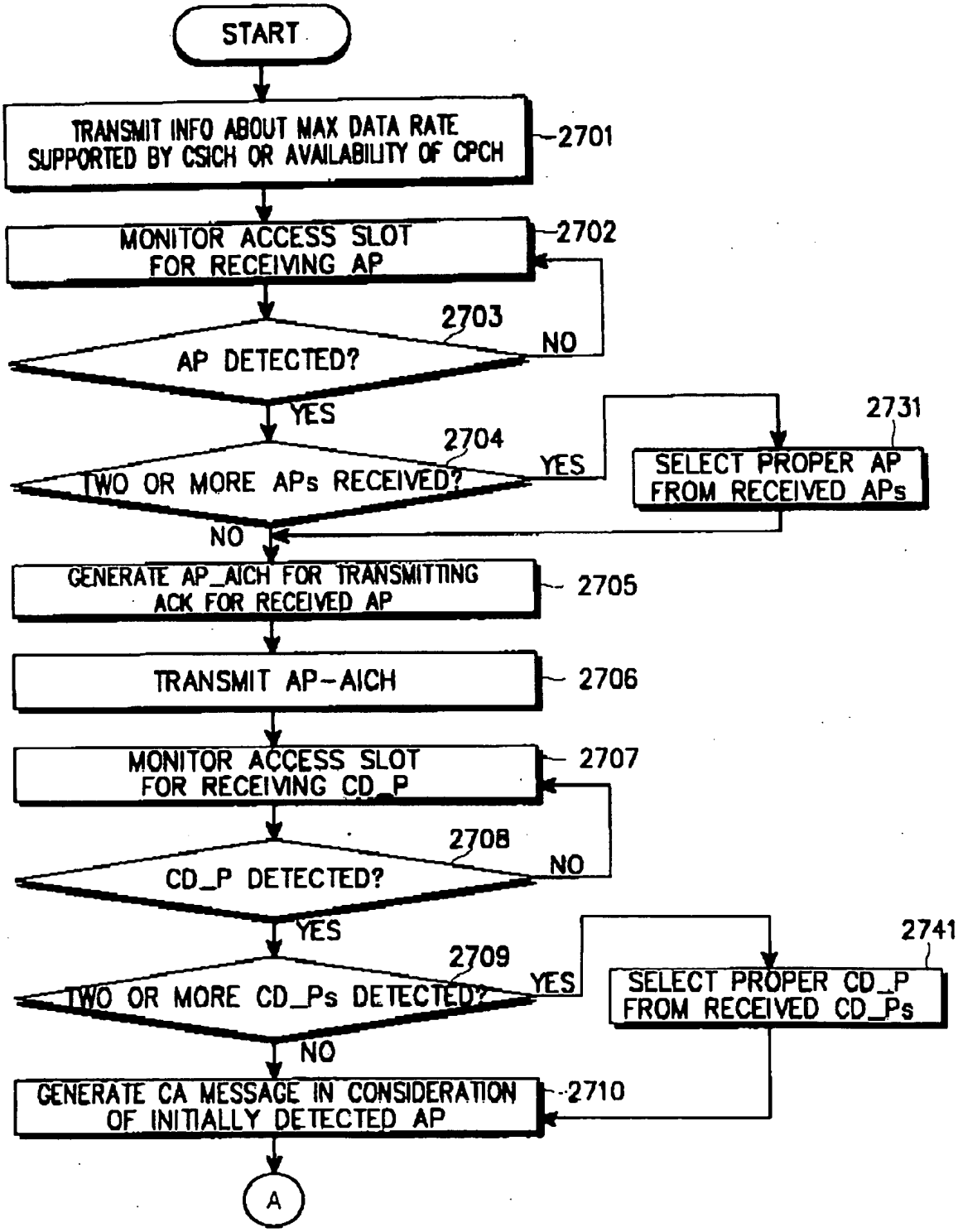

START
TRANSMIT INFO ABOUT MAX DATA RATE SUPPORTED BY CSICH OR AVAILABILITY OF CPCH
2701
MONITOR ACCESS SLOT FOR RECEIVING AP
2702
2703
AP DETECTED?
NO
YES
2731
2704
TWO OR MORE APs RECEIVED?
YES
SELECT PROPER AP FROM RECEIVED APs
NO
GENERATE AP_AICH FOR TRANSMITTING ACK FOR RECEIVED AP
2705
TRANSMIT AP-AICH
2706
MONITOR ACCESS SLOT FOR RECEIVING CD_P
2707
2708
CD_P DETECTED?
NO
YES
2741
2709
TWO OR MORE CD_Ps DETECTED?
YES
SELECT PROPER CD_P FROM RECEIVED CD_Ps
NO
GENERATE CA MESSAGE IN CONSIDERATION OF INITIALLY DETECTED AP
2710
A

FIG. 27A

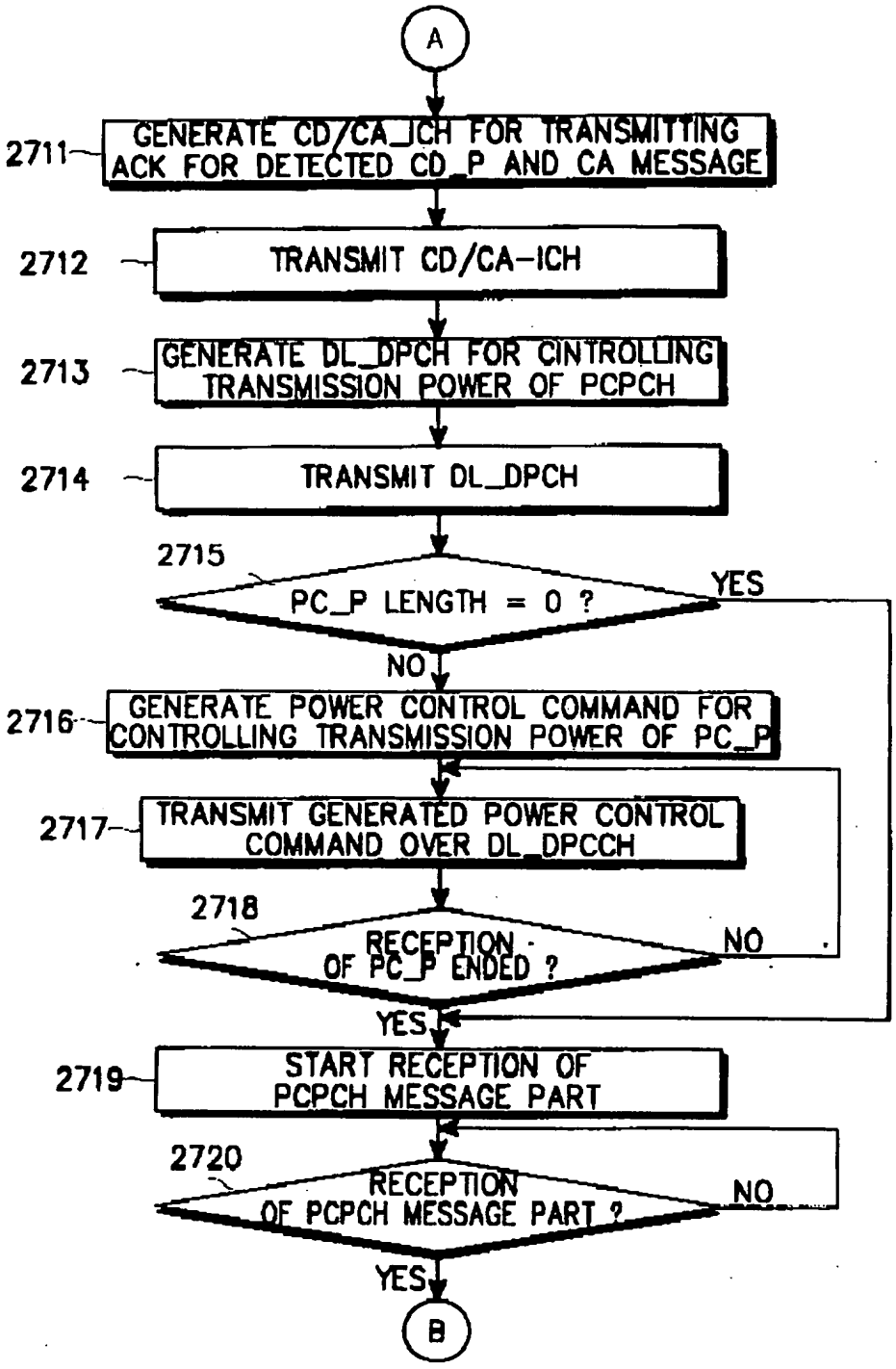

A
2711
GENERATE CD/CA_ICH FOR TRANSMITTING ACK FOR DETECTED CD_P AND CA MESSAGE
2712
TRANSMIT CD/CA-ICH
2713
GENERATE DL_DPCH FOR CINTROLLING TRANSMISSION POWER OF PCPCH
2714
TRANSMIT DL_DPCH
2715
PC_P LENGTH = 0 ?
YES
NO
2716
GENERATE POWER CONTROL COMMAND FOR CONTROLLING TRANSMISSION POWER OF PC_P
2717
TRANSMIT GENERATED POWER CONTROL COMMAND OVER DL_DPCCH
2718
RECEPTION OF PC_P ENDED ?
NO
YES
2719
START RECEPTION OF PCPCH MESSAGE PART
2720
RECEPTION OF PCPCH MESSAGE PART ?
NO
YES
B

FIG. 27B

FLOWCHART OF CPCH USING CHANNEL ASSIGNMENT
(UTRAN SIDE)

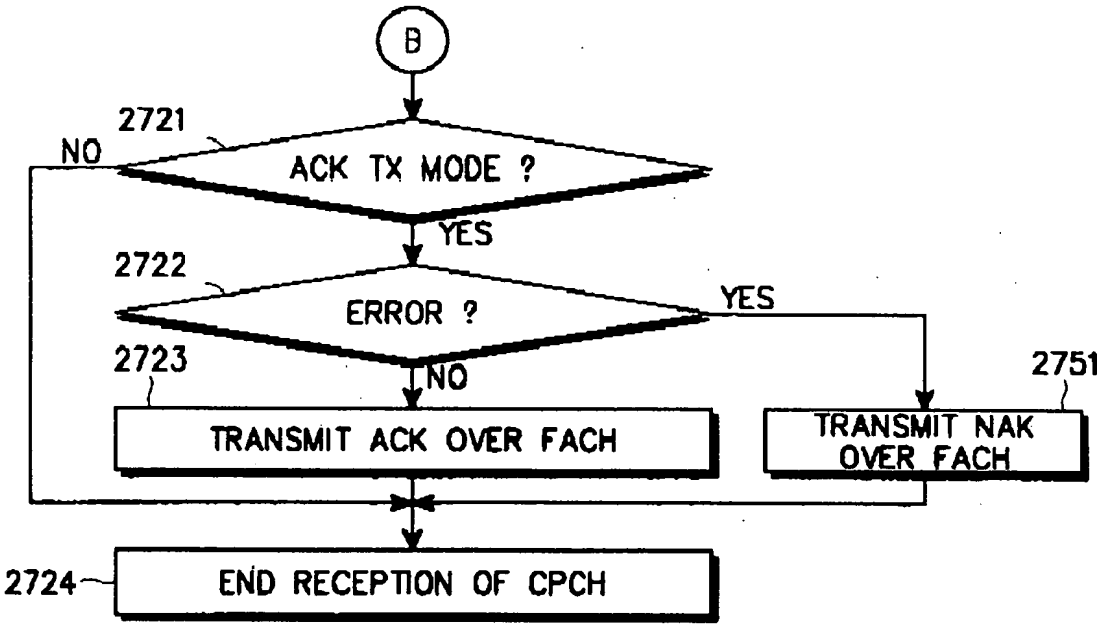


FIG. 27C

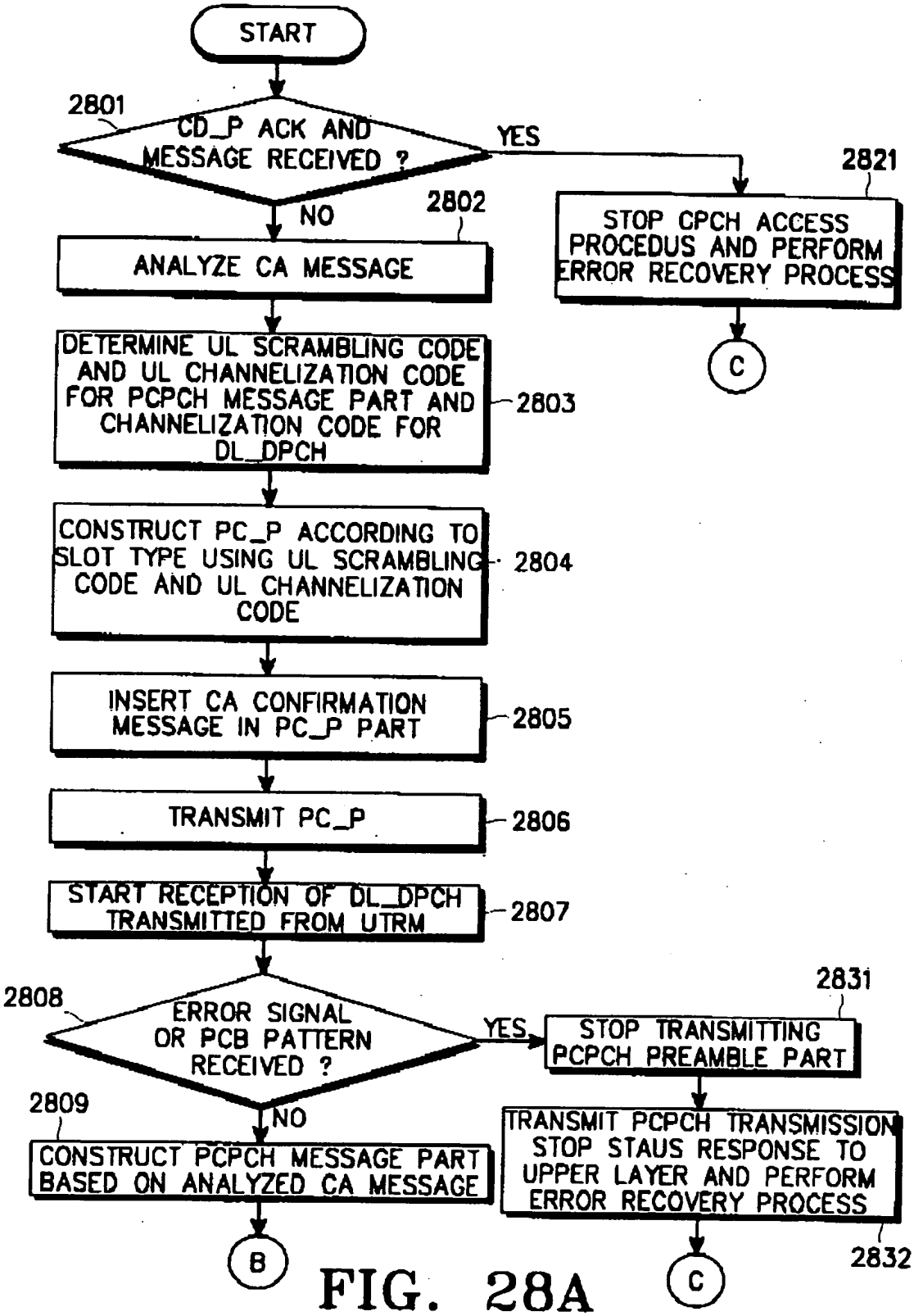

START
2801
CD_P ACK AND MESSAGE RECEIVED ?
YES
2821
STOP CPCH ACCESS PROCEDUS AND PERFORM ERROR RECOVERY PROCESS
C
NO
2802
ANALYZE CA MESSAGE
DETERMINE UL SCRAMBLING CODE AND UL CHANNELIZATION CODE FOR PCPCH MESSAGE PART AND CHANNELIZATION CODE FOR DL_DPCH
2803
CONSTRUCT PC_P ACCORDING TO SLOT TYPE USING UL SCRAMBLING CODE AND UL CHANNELIZATION CODE
2804
INSERT CA CONFIRMATION MESSAGE IN PC_P PART
2805
TRANSMIT PC_P
2806
START RECEPTION OF DL_DPCH TRANSMITTED FROM UTRM
2807
2808
ERROR SIGNAL OR PCB PATTERN RECEIVED ?
YES
2831
STOP TRANSMITTING PCPCH PREAMBLE PART
TRANSMIT PCPCH TRANSMISSION STOP STAUS RESPONSE TO UPPER LAYER AND PERFORM ERROR RECOVERY PROCESS
2832
C
2809
NO
CONSTRUCT PCPCH MESSAGE PART BASED ON ANALYZED CA MESSAGE
B

FIG. 28A

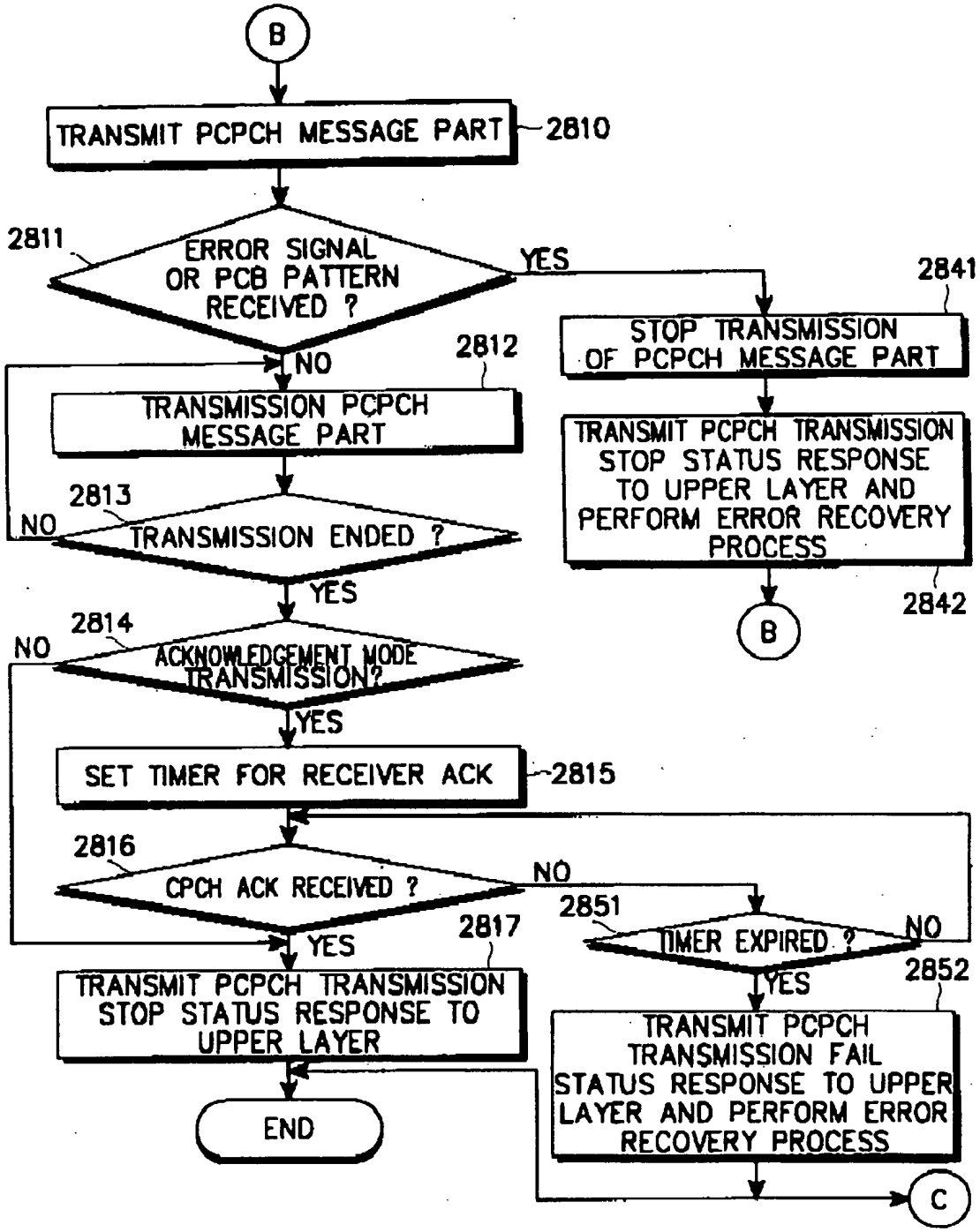

B
TRANSMIT PCPCH MESSAGE PART
2810
2811
ERROR SIGNAL OR PCB PATTERN RECEIVED ?
YES
2841
STOP TRANSMISSION OF PCPCH MESSAGE PART
NO
2812
TRANSMISSION PCPCH MESSAGE PART
TRANSMIT PCPCH TRANSMISSION STOP STATUS RESPONSE TO UPPER LAYER AND PERFORM ERROR RECOVERY PROCESS
2813
NO
TRANSMISSION ENDED ?
YES
2842
B
2814
NO
ACKNOWLEDGEMENT MODE TRANSMISSION?
YES
SET TIMER FOR RECEIVER ACK
2815
2816
CPCH ACK RECEIVED ?
NO
2851
TIMER EXPIRED ?
NO
YES
2817
YES
2852
TRANSMIT PCPCH TRANSMISSION STOP STATUS RESPONSE TO UPPER LAYER
TRANSMIT PCPCH TRANSMISSION FAIL STATUS RESPONSE TO UPPER LAYER AND PERFORM ERROR RECOVERY PROCESS
END
C

FIG. 28B

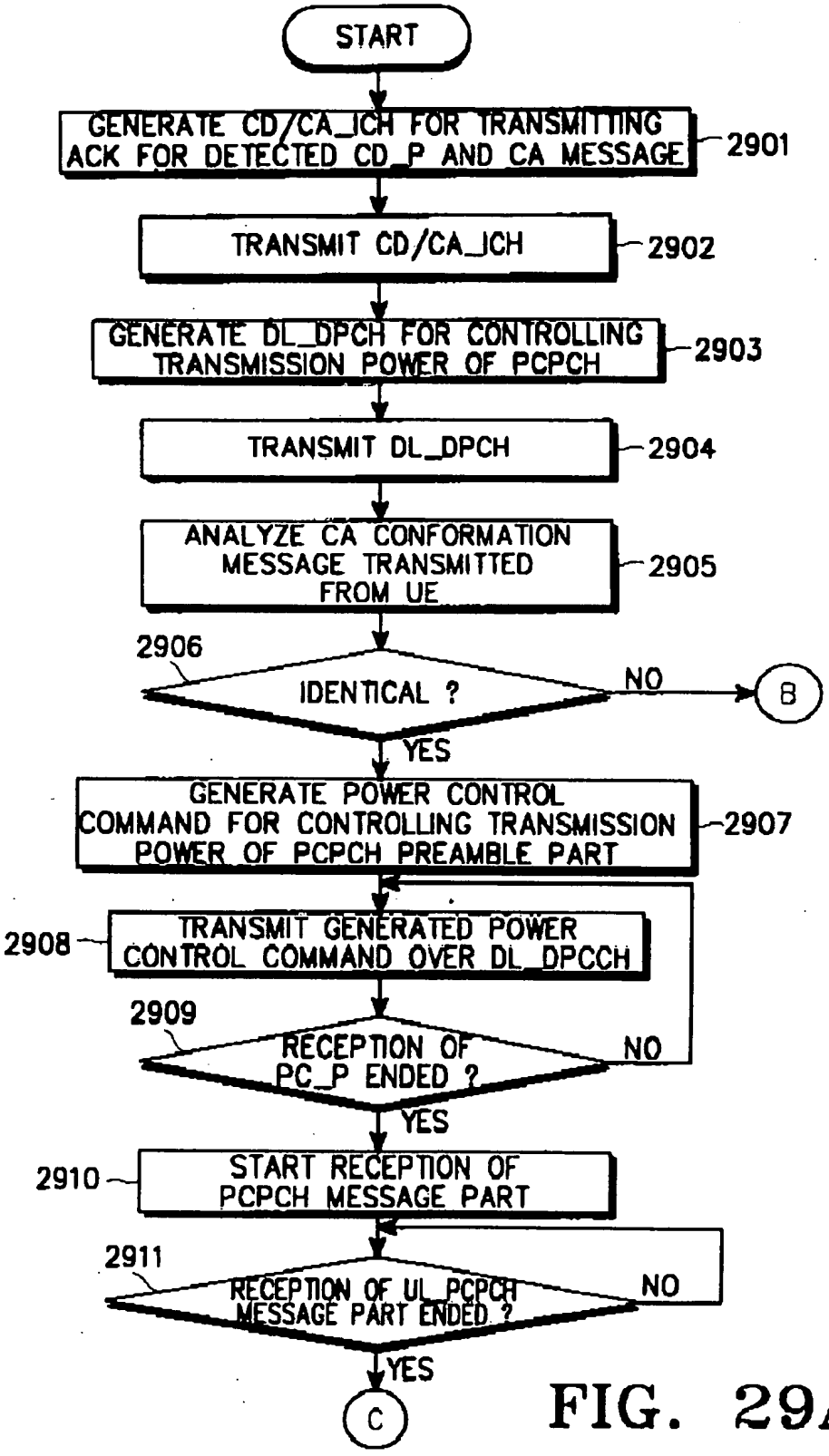

START
GENERATE CD/CA_ICH FOR TRANSMITTING ACK FOR DETECTED CD_P AND CA MESSAGE
2901
TRANSMIT CD/CA_ICH
2902
GENERATE DL_DPCH FOR CONTROLLING TRANSMISSION POWER OF PCPCH
2903
TRANSMIT DL_DPCH
2904
ANALYZE CA CONFORMATION MESSAGE TRANSMITTED FROM UE
2905
2906
IDENTICAL ?
NO
B
YES
GENERATE POWER CONTROL COMMAND FOR CONTROLLING TRANSMISSION POWER OF PCPCH PREAMBLE PART
2907
2908
TRANSMIT GENERATED POWER CONTROL COMMAND OVER DL_DPCCH
2909
RECEPTION OF PC_P ENDED ?
NO
YES
2910
START RECEPTION OF PCPCH MESSAGE PART
2911
RECEPTION OF UL_PCPCH MESSAGE PART ENDED ?
NO
YES
C

FIG. 29A

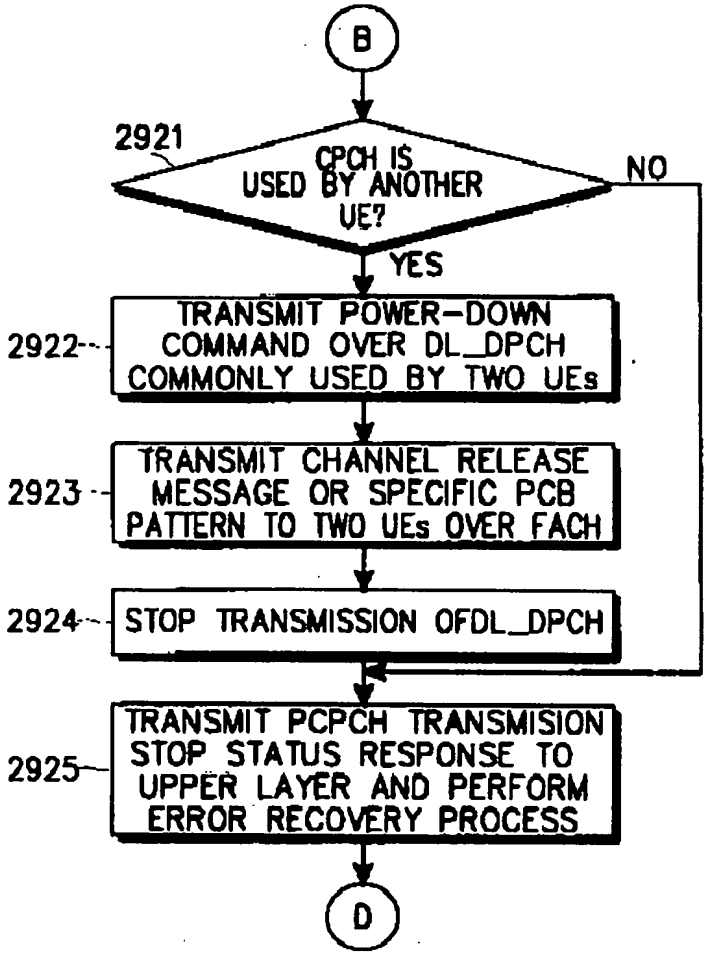

B
2921
CPCH IS USED BY ANOTHER UE?
NO
YES
2922
TRANSMIT POWER-DOWN COMMAND OVER DL_DPCH COMMONLY USED BY TWO UEs
2923
TRANSMIT CHANNEL RELEASE MESSAGE OR SPECIFIC PCB PATTERN TO TWO UEs OVER FACH
2924
STOP TRANSMISSION OFDL_DPCH
2925
TRANSMIT PCPCH TRANSMISION STOP STATUS RESPONSE TO UPPER LAYER AND PERFORM ERROR RECOVERY PROCESS
D

FIG. 29B

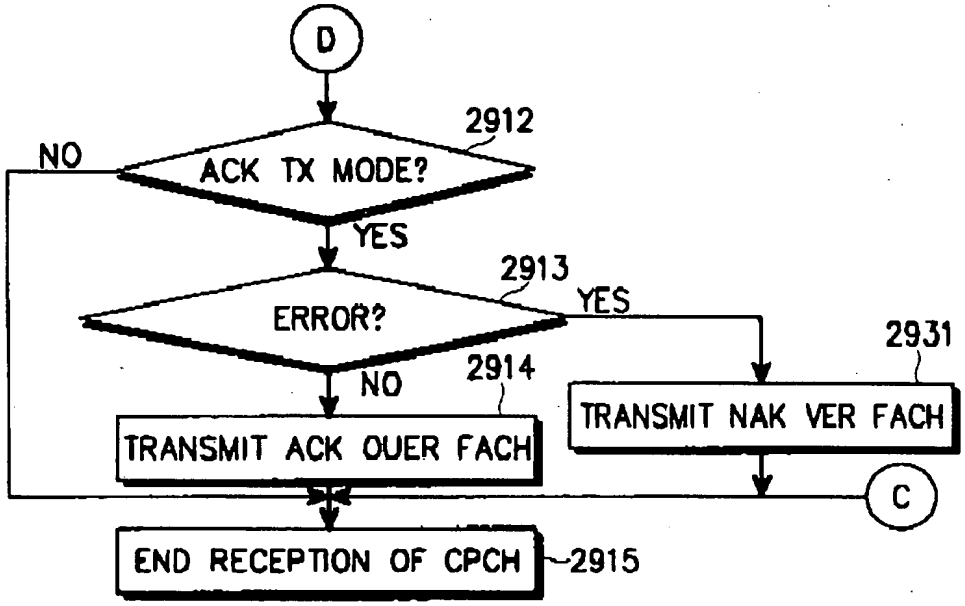

D
2912
NO
ACK TX MODE?
YES
2913
ERROR?
YES
2931
NO
2914
TRANSMIT NAK VER FACH
TRANSMIT ACK OUER FACH
C
END RECEPTION OF CPCH
2915

FIG. 29C

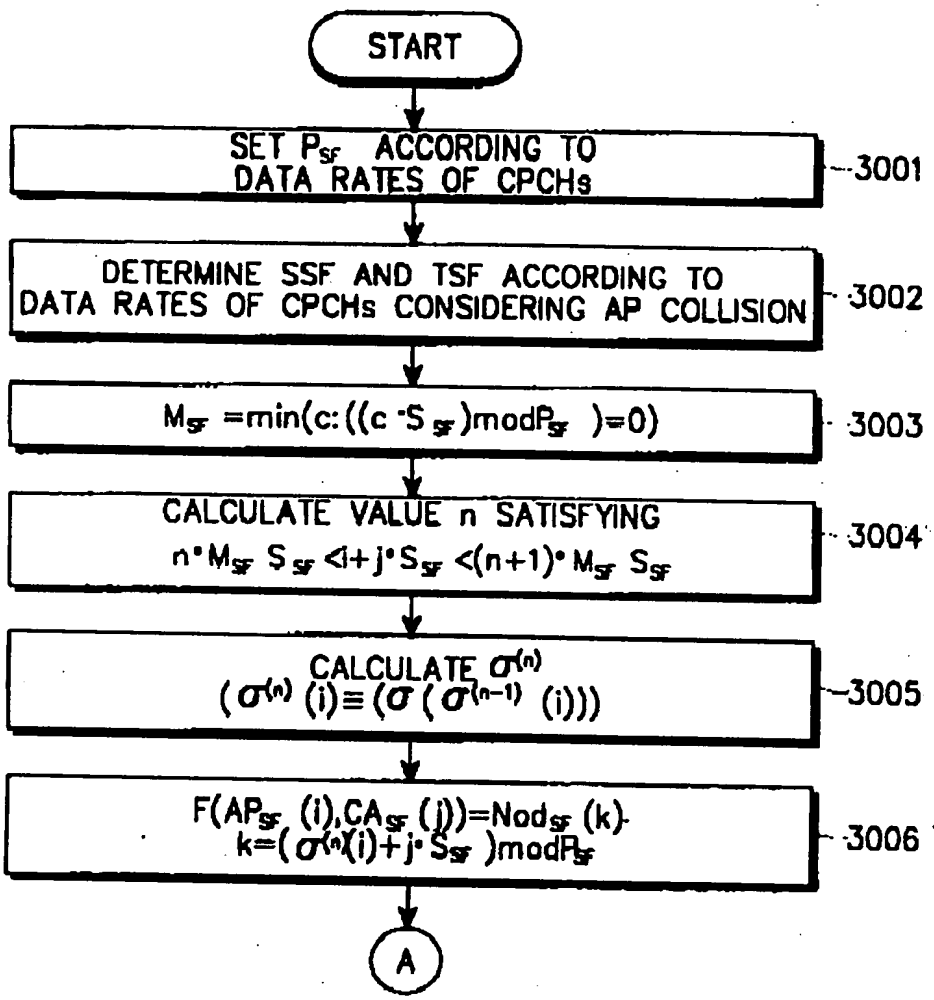

START
SET P_{SF} ACCORDING TO DATA RATES OF CPCHs
3001
DETERMINE SSF AND TSF ACCORDING TO DATA RATES OF CPCHs CONSIDERING AP COLLISION
3002
M_{SF} =min(c:((c·S_{SF})modP_{SF})=0)
3003
CALCULATE VALUE n SATISFYING
$n \cdot M_{SF}\ S_{SF} < i + j \cdot S_{SF} < (n+1) \cdot M_{SF}\ S_{SF}$
3004
CALCULATE $\sigma^{(n)}$
$(\sigma^{(n)}(i) \equiv (\sigma(\sigma^{(n-1)}(i)))$
3005
$F(AP_{SF}(i), CA_{SF}(j)) = Nod_{SF}(k)$
$k = (\sigma^{(n)}(i) + j \cdot S_{SF})\ mod P_{SF}$
3006
A

FIG. 30A

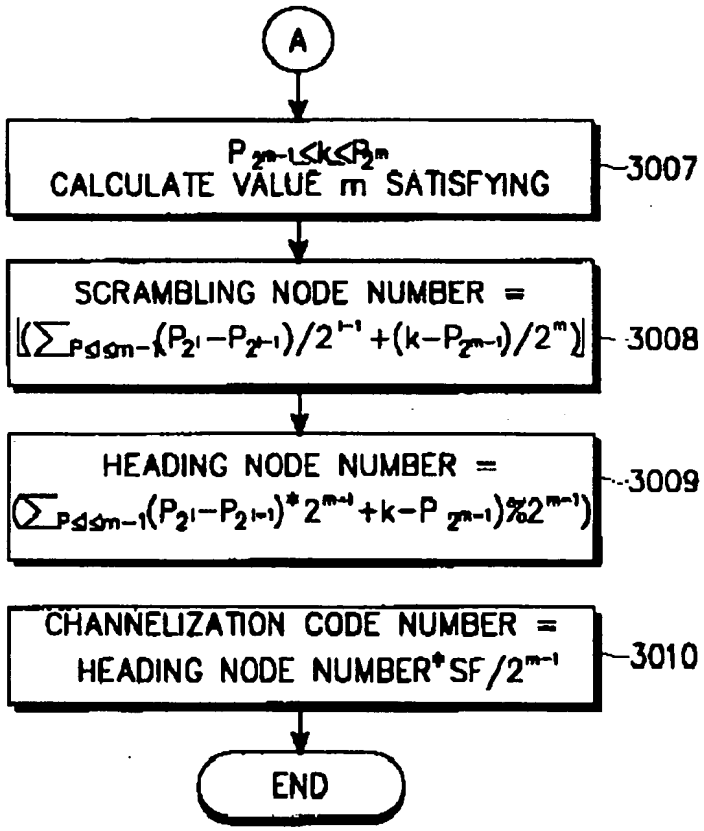

A
$P_{2^{m-1}} \le k < P_{2^m}$
CALCULATE VALUE m SATISFYING
3007
SCRAMBLING NODE NUMBER =
$\lfloor (\sum_{P \le 2^{m-1}} (P_{2^l} - P_{2^{l-1}})/2^{l-1} + (k - P_{2^{m-1}})/2^m) \rfloor$
3008
HEADING NODE NUMBER =
$(\sum_{P \le 2^{m-1}} (P_{2^l} - P_{2^{l-1}}) * 2^{m-1} + k - P_{2^{m-1}}) \% 2^{m-1})$
3009
CHANNELIZATION CODE NUMBER =
HEADING NODE NUMBER * SF / 2^{m-1}
3010
END

FIG. 30B

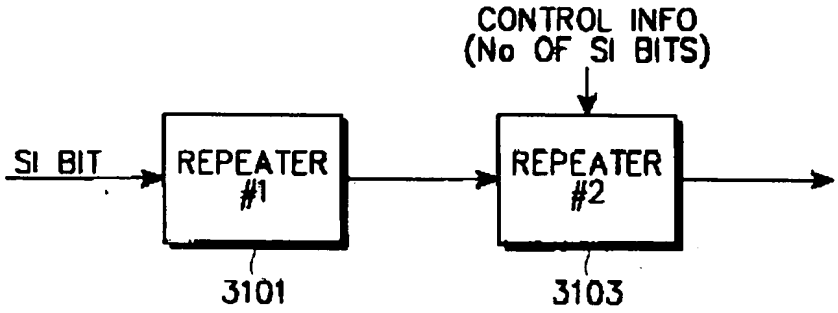

CONTROL INFO
(No OF SI BITS)
SI BIT
REPEATER
#1
REPEATER
#2
3101
3103

FIG. 31

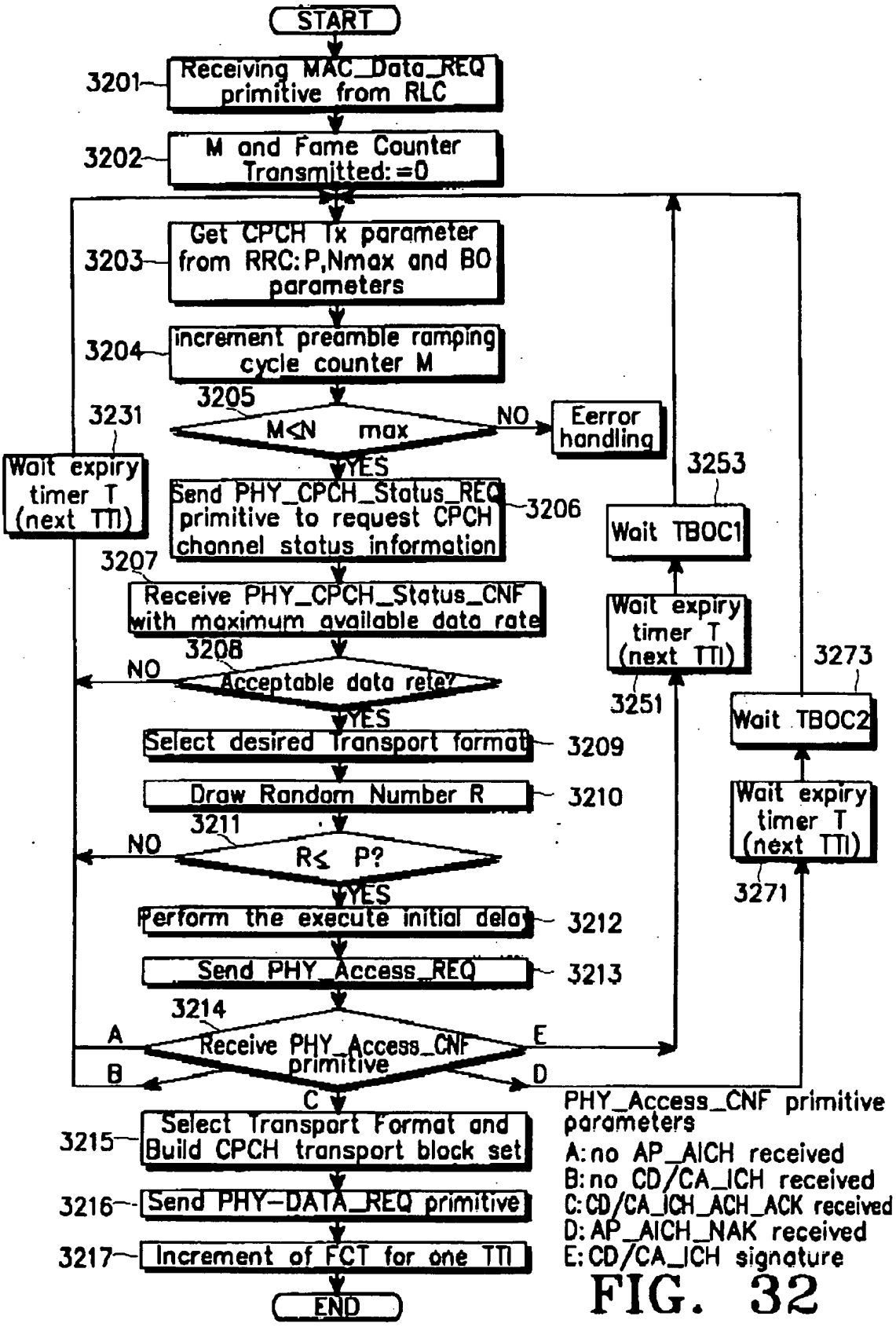

START
3201
Receiving MAC_Data_REQ primitive from RLC
3202
M and Fame Counter Transmitted: =0
3203
Get CPCH Tx parameter from RRC: P,Nmax and BO parameters
3204
increment preamble ramping cycle counter M
3205
M<N max
NO
Eerror handling
YES
3231
Wait expiry timer T (next TTI)
Send PHY_CPCH_Status_REQ primitive to request CPCH channel status information
3206
3207
Receive PHY_CPCH_Status_CNF with maximum available data rate
3208
Acceptable data rate?
NO
YES
Select desired Transport format
3209
Draw Random Number R
3210
3211
R≤ P?
NO
YES
Perform the execute initial delay
3212
Send PHY_Access_REQ
3213
3214
Receive PHY_Access_CNF primitive
A
B
C
D
E
3215
Select Transport Format and Build CPCH transport block set
3216
Send PHY-DATA_REQ primitive
3217
Increment of FCT for one TTI
END
3253
Wait TBOC1
Wait expiry timer T (next TTI)
3251
3273
Wait TBOC2
Wait expiry timer T (next TTI)
3271
PHY_Access_CNF primitive parameters
A: no AP_AICH received
B: no CD/CA_ICH received
C: CD/CA_ICH_ACH_ACK received
D: AP_AICH_NAK received
E: CD/CA_ICH signature

FIG. 32

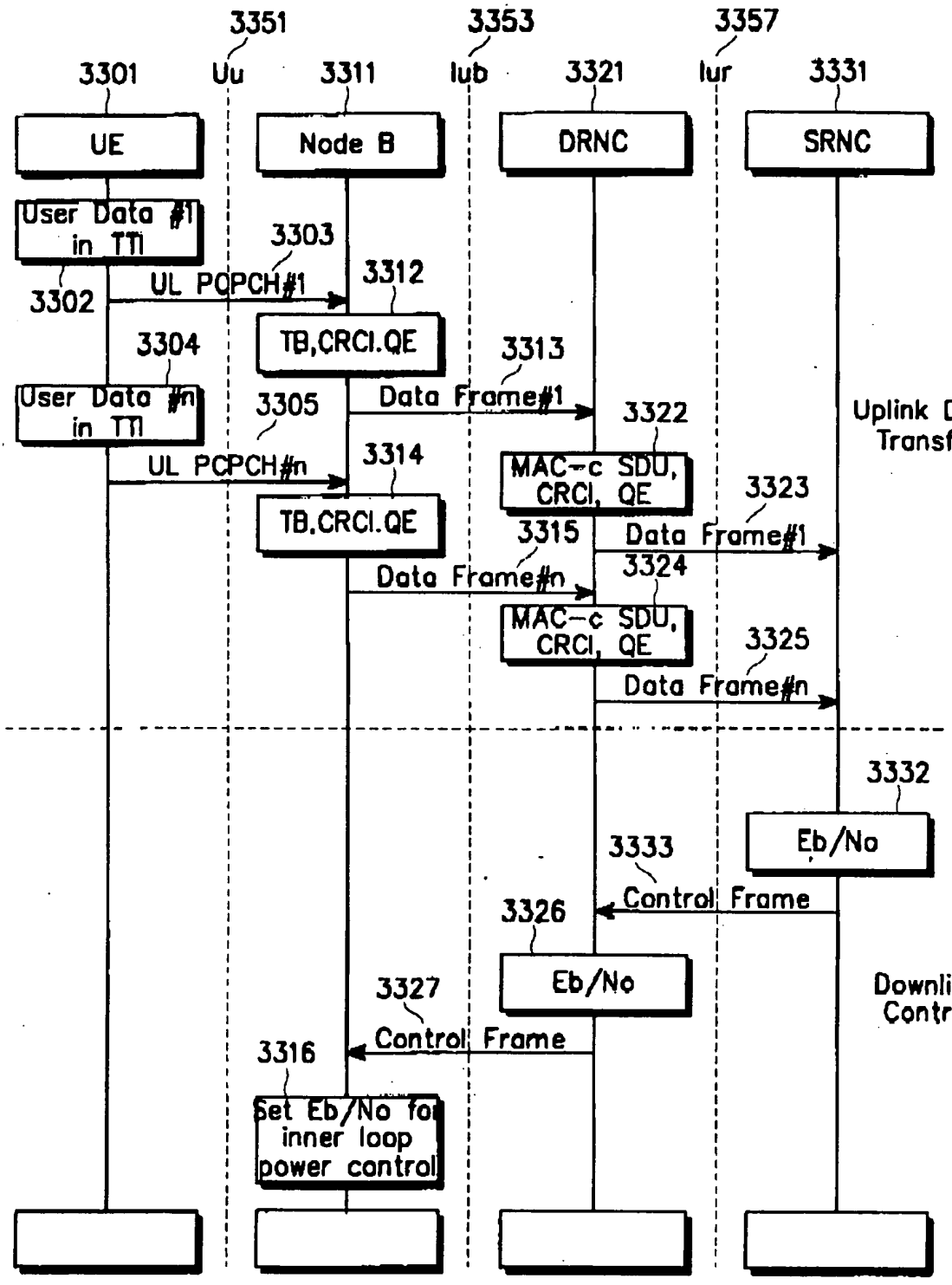

3351
3353
3357
3301
Uu
3311
Iub
3321
Iur
3331
UE
Node B
DRNC
SRNC
User Data #1 in TTI
3303
3302
UL PCPCH#1
3312
TB,CRCI,QE
3304
3313
User Data #n in TTI
Data Frame#1
3322
Uplink Data Transfer
3305
UL PCPCH#n
3314
MAC-c SDU, CRCI, QE
3323
TB,CRCI,QE
3315
Data Frame#1
Data Frame#n
3324
MAC-c SDU, CRCI, QE
3325
Data Frame#n
3332
Eb/No
3333
Control Frame
3326
Eb/No
Downlink Control
3327
Control Frame
3316
Set Eb/No for inner loop power control

FIG. 33

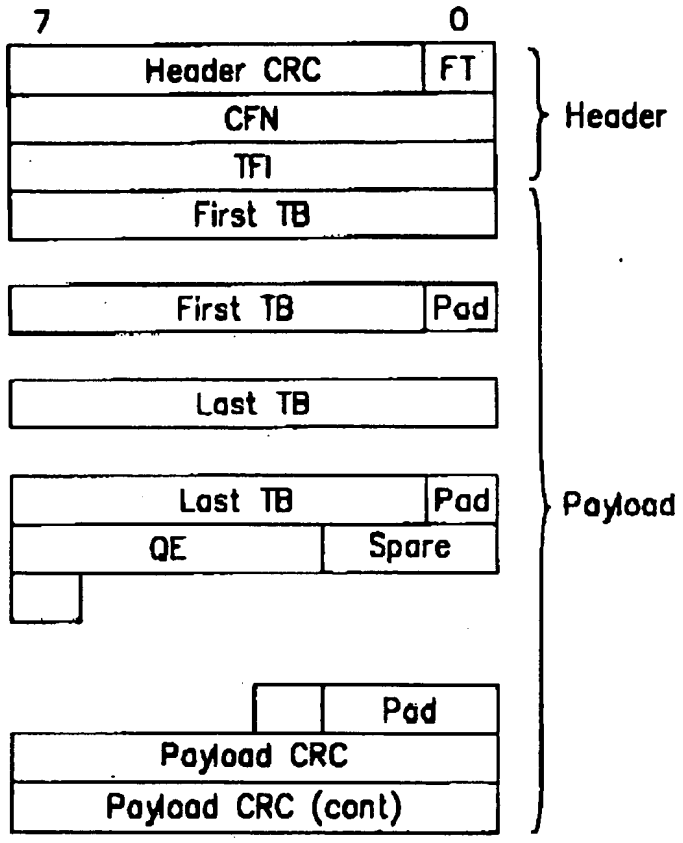

7
0
Header CRC
FT
CFN
TFI
First TB
Header
First TB
Pad
Last TB
Last TB
Pad
QE
Spare
Pad
Payload CRC
Payload CRC (cont)
Payload

FIG. 34

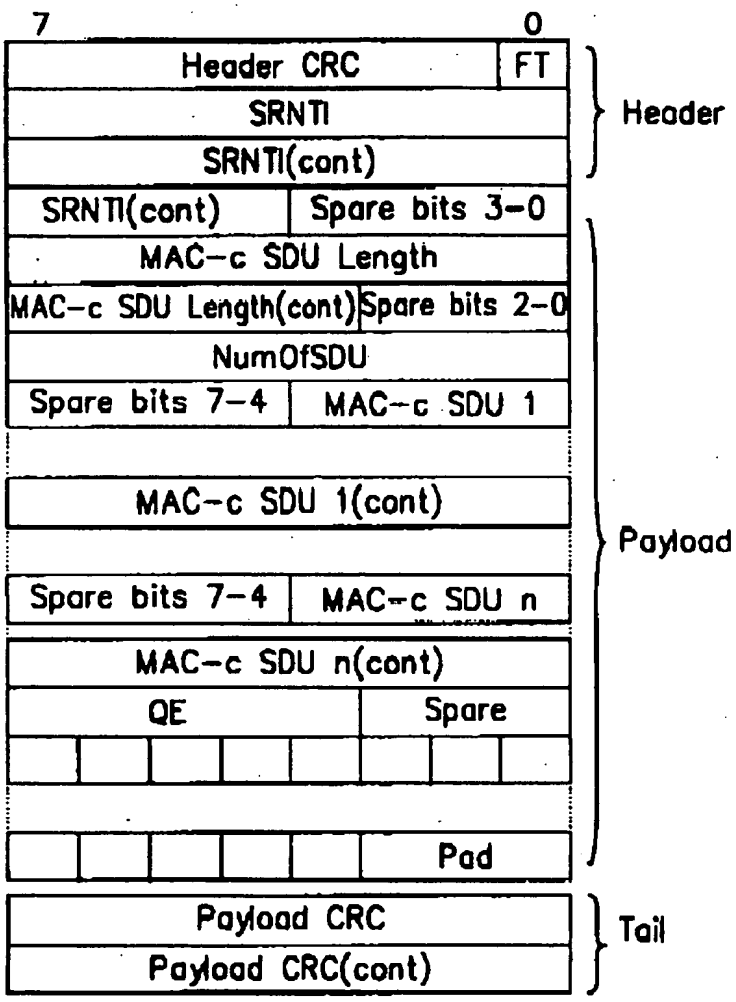

7
0
Header CRC
FT
SRNTI
SRNTI(cont)
SRNTI(cont)
Spare bits 3-0
MAC-c SDU Length
MAC-c SDU Length(cont)
Spare bits 2-0
NumOfSDU
Spare bits 7-4
MAC-c SDU 1
MAC-c SDU 1(cont)
Spare bits 7-4
MAC-c SDU n
MAC-c SDU n(cont)
QE
Spare
Pad
Payload CRC
Payload CRC(cont)
Header
Payload
Tail

FIG. 35

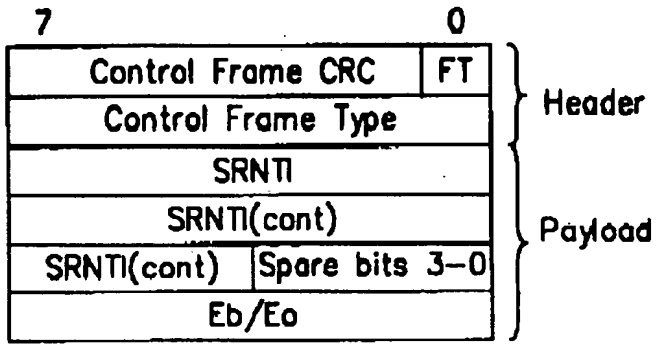

7
0
Control Frame CRC
FT
Control Frame Type
SRNTI
SRNTI(cont)
SRNTI(cont)
Spare bits 3-0
Eb/Eo
Header
Payload

FIG. 36

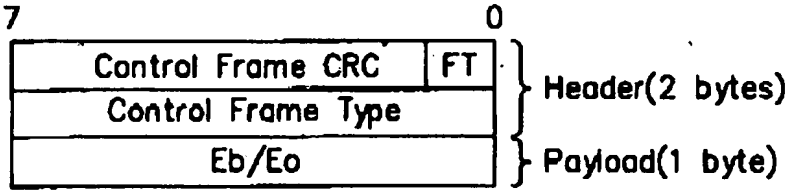

7
0
Control Frame CRC
FT
Control Frame Type
Eb/Eo
Header(2 bytes)
Payload(1 byte)

FIG. 37